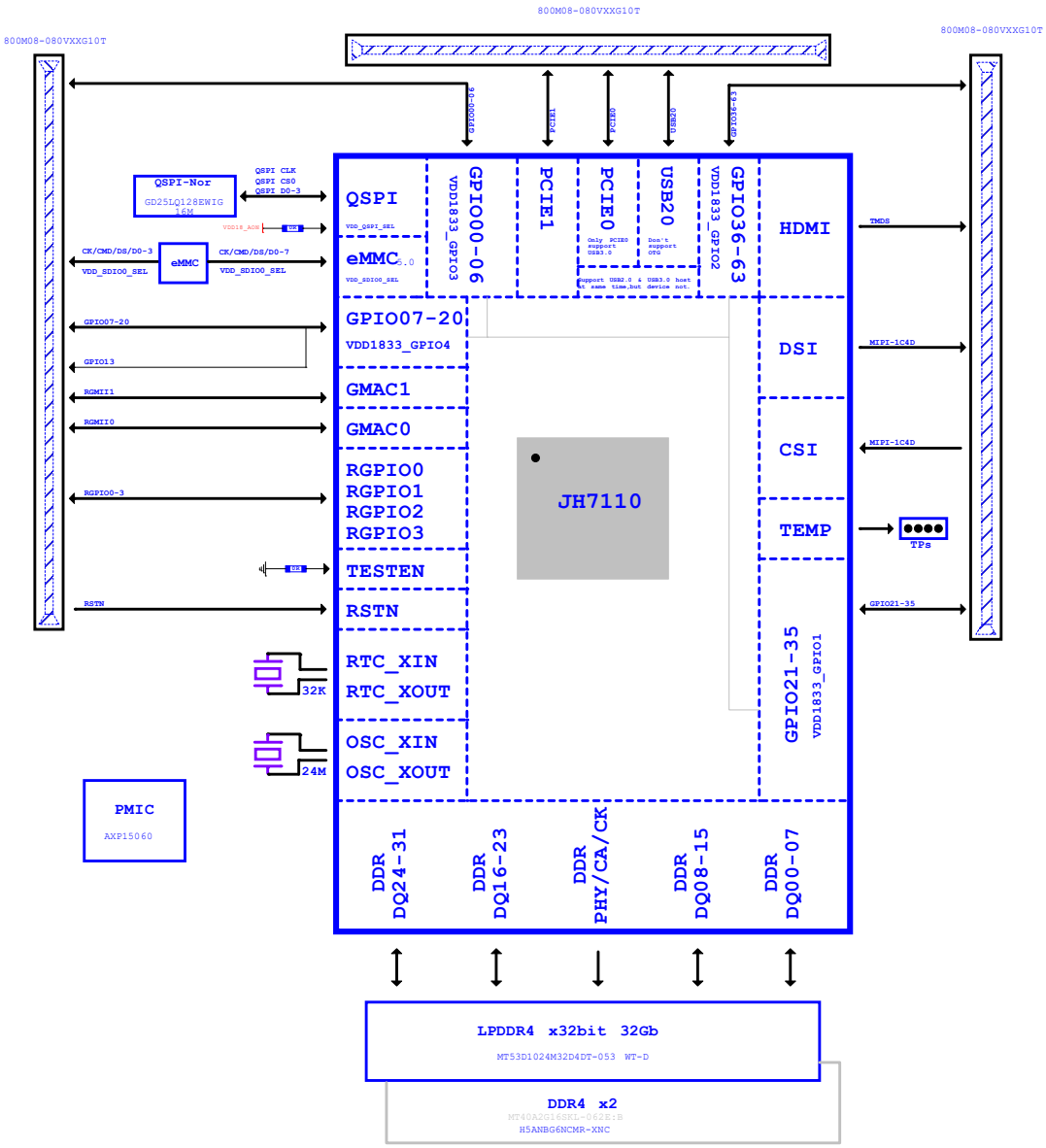

Core Board

StarFive 赛昉科技		
Title: JH7110_Devkit_LP4		
Size: C	Document Number: 01.Diagram-Core Sys	Rev: V10
Date: Wednesday, July 26, 2023	Sheet 1 of 16	

Main Board

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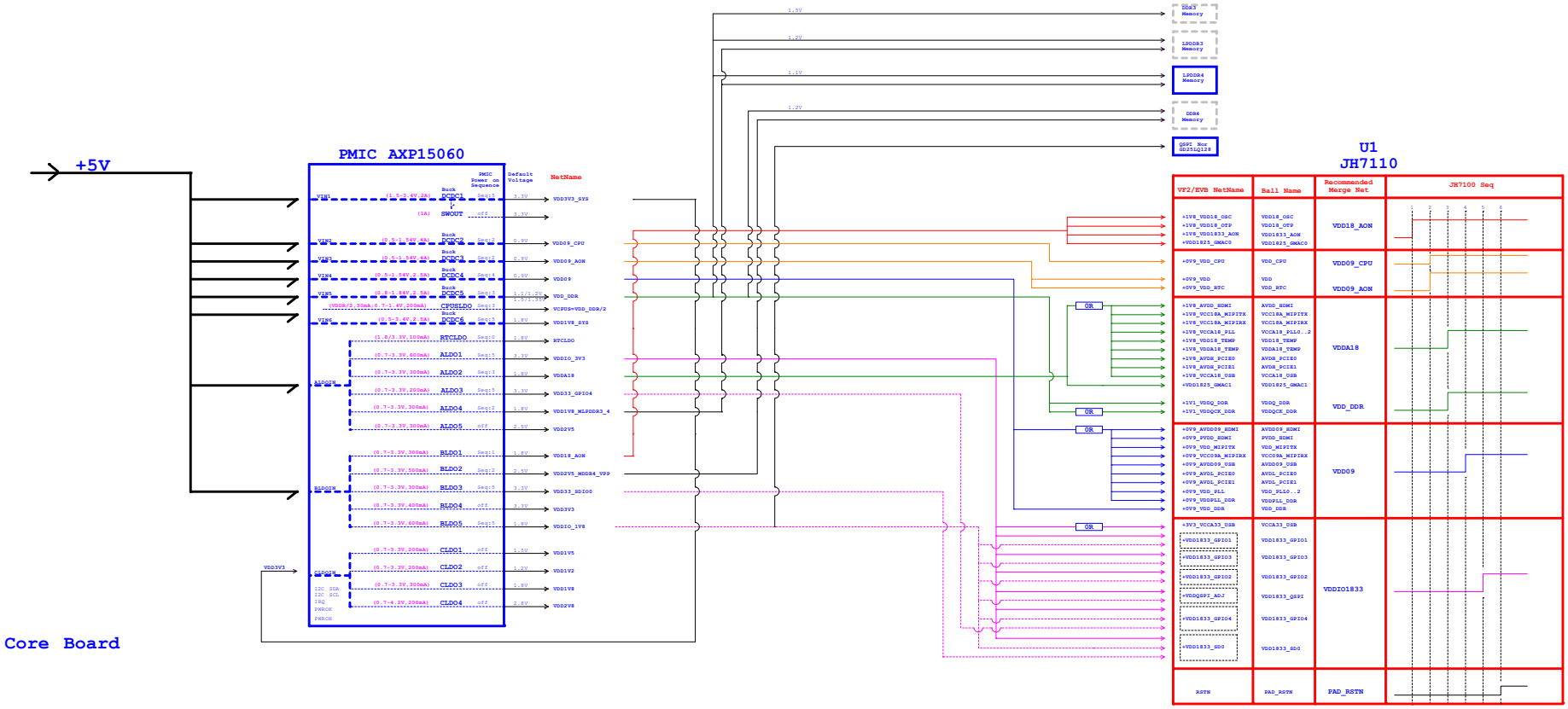
Title	JH7110_Devkit_LP4		
Size: B	Document Number: 02:Diagram-MainIO		Rev: V10
Date: Wednesday, July 26, 2023	Sheet 2 of 16		



Title	JH7110_Devkit_LP4		
Size C	Document Number 03:Diagram PD		Rev V10
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PAGE LIST

JH7110 GPIO List

Power Group	GPIO Name	Default FUN	Core Devices	Main Devices	Notes
VDD1833_GPIO3	GPIO00				
	GPIO01				
	GPIO02				
	GPIO03				
	GPIO04				
	GPIO05				
	GPIO06				
VDD1833_GPIO4	GPIO07				
	GPIO08				
	GPIO09				
	GPIO10				
	GPIO11				
	GPIO12				
	GPIO13				
	GPIO14				
	GPIO15				
	GPIO16				
	GPIO17				
	GPIO18				
	GPIO19	PMIC_SCK/E2PROM_SCK	U10 & U14		
	GPIO20	PMIC_SDA/E2PROM_SDA	U10 & U14		
VDD1833_GPIO1	GPIO21	DDR Type/Size Config			
	GPIO22	DDR Type/Size Config			
	GPIO23	DDR Type/Size Config			
	GPIO24	DDR Type/Size Config			
	GPIO25				
	GPIO26				
	GPIO27				
	GPIO28				
	GPIO29				
	GPIO30				
	GPIO31				
	GPIO32				
	GPIO33				
	GPIO34				
	GPIO35				
VDD1833_GPIO2	GPIO36				
	GPIO37				
	GPIO38				
	GPIO39				
	GPIO40				
	GPIO41				
	GPIO42				
	GPIO43				
	GPIO44				
	GPIO45				
	GPIO46				
	GPIO47				
	GPIO48				
	GPIO49				
	GPIO50				
	GPIO51				
	GPIO52				
	GPIO53				
	GPIO54				
	GPIO55				
	GPIO56				
	GPIO57				
	GPIO58				
	GPIO59				
	GPIO60				
	GPIO61				
	GPIO62	SDMMC_RST_N	U7		
	GPIO63				
VDD18_AON	RGPIO0	Boot Mode			
	RGPIO1	Boot Mode			
	RGPIO2	Boot Mode			

Note1: All 64GPIOs support full mux,Please refer to relevant detailed documents.

Note2: "- - - - - << NetName" or "NetName <<- -" is only used to indicate the connection between pages.

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Title	JH7110 Devkit_LP4	
Size: B	Document Number: 04:Diagram GPIOs List	Rev: V10
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JH7110_DEVKIT_LPDDR4_CORE_L6_V10:

20230416A update to 20230517A:

1.Update descrition about LPDDR4 Size(GPIO22,21=11:TBD→ 1GB) on page10;
2.Change Pull-uped resistor of "SDMMC_CMD" R195 4.7K to 1.5k on page14;
3.Change R208,Q2,R506 to NC on page14;
4.Add costdown solution for "VDD1833_SPI01/2/3/4 Fixed to 3.3V on page16;

20230517A update to 20230601A:

1.Modefy net names of J1_PIN74,76 80 on page5
2.Change R520,521,522,523,524 to NC on page10;

V10 20230601A update to V11 20230701 :

1.Update JH7110 reset circuits on page16;
(the reset circuits are not updated to PCB and BOM)

V11 20230701 update to V20 20230726 :

1.Update JH7110 reset circuits on page16;

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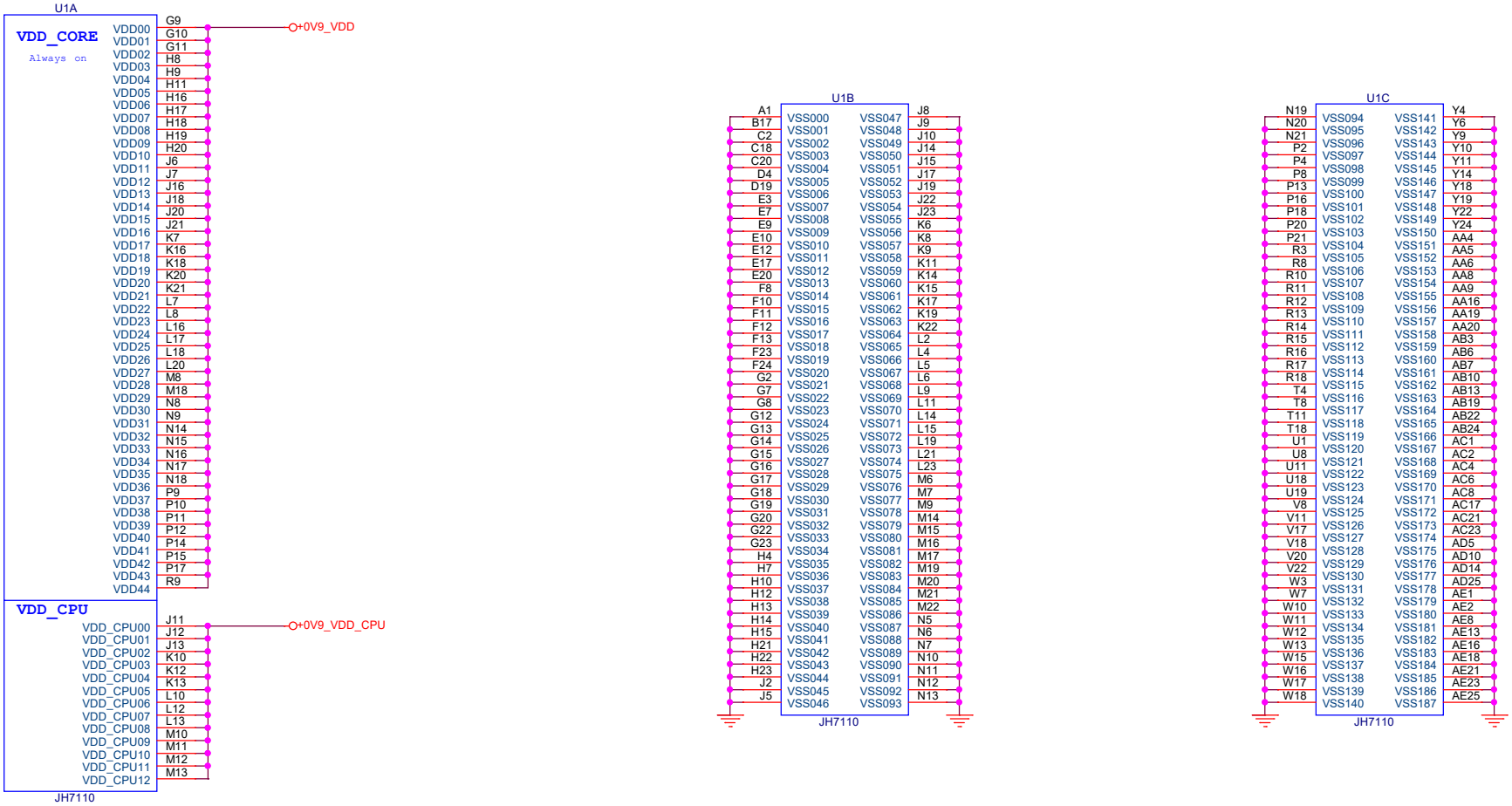
Title	JH7110 Devkit_LP4		
Size B	Document Number 05:History		Rev V10
Date: Wednesday, July 26, 2023	Sheet 5 of 16		



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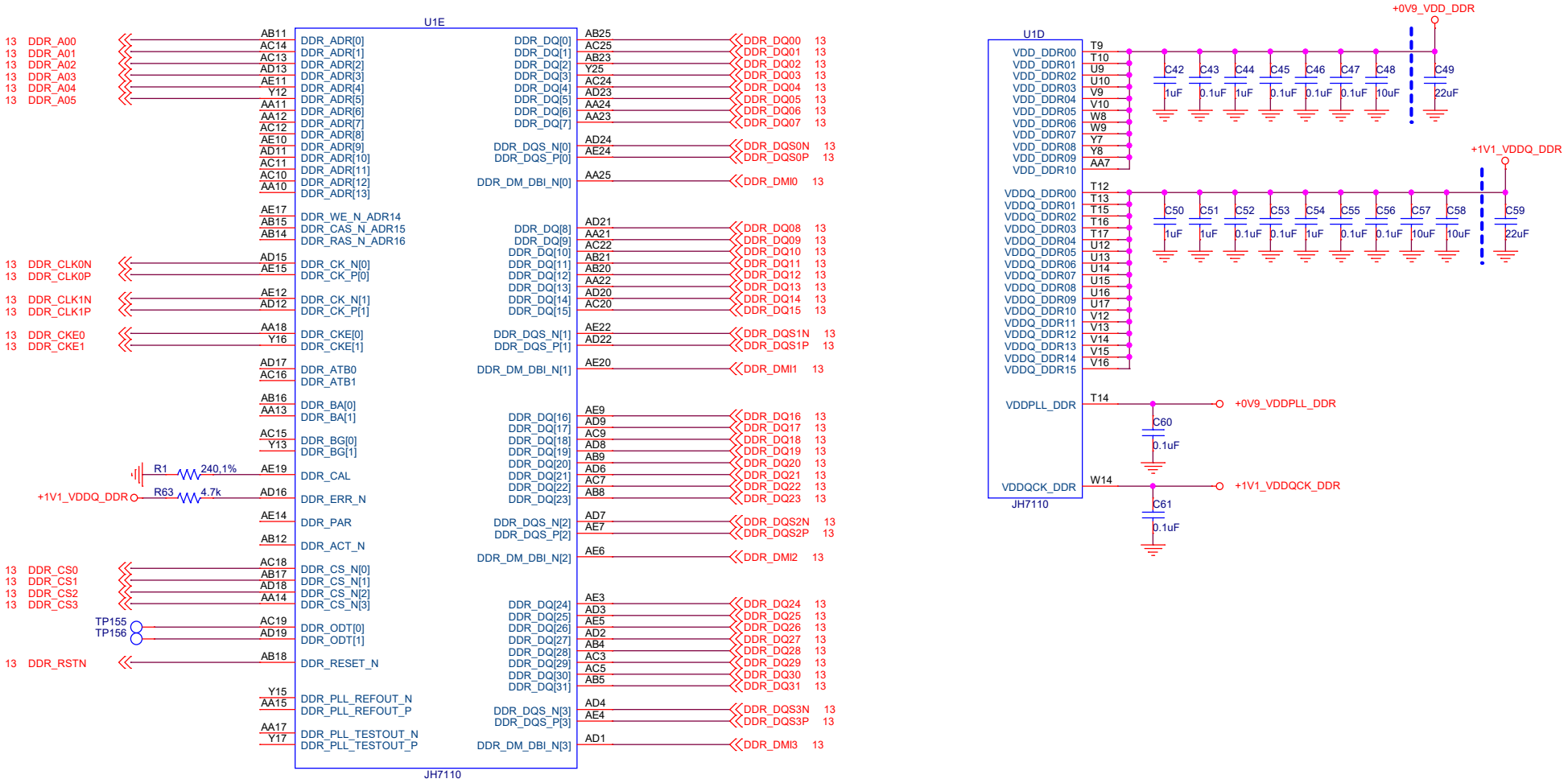
Title	JH7110 Devkit_LP4	
Size B	Document Number 06:JH7110 Power	Rev V10
Date: Wednesday, July 26, 2023	Sheet 6 of 16	



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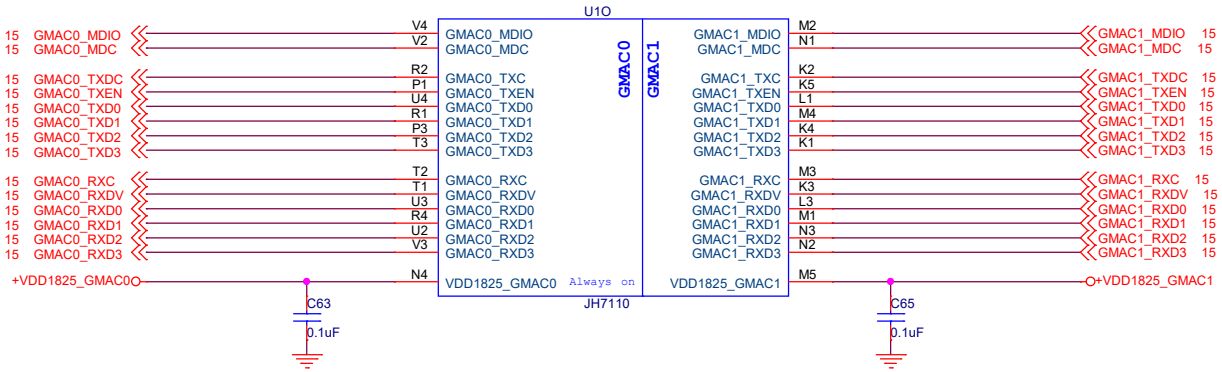
Title	JH7110 Devkit_LP4	
Size B	Document Number 07:JH7110 DDR Ctrl	Rev V10
Date: Wednesday, July 26, 2023	Sheet 7 of 16	



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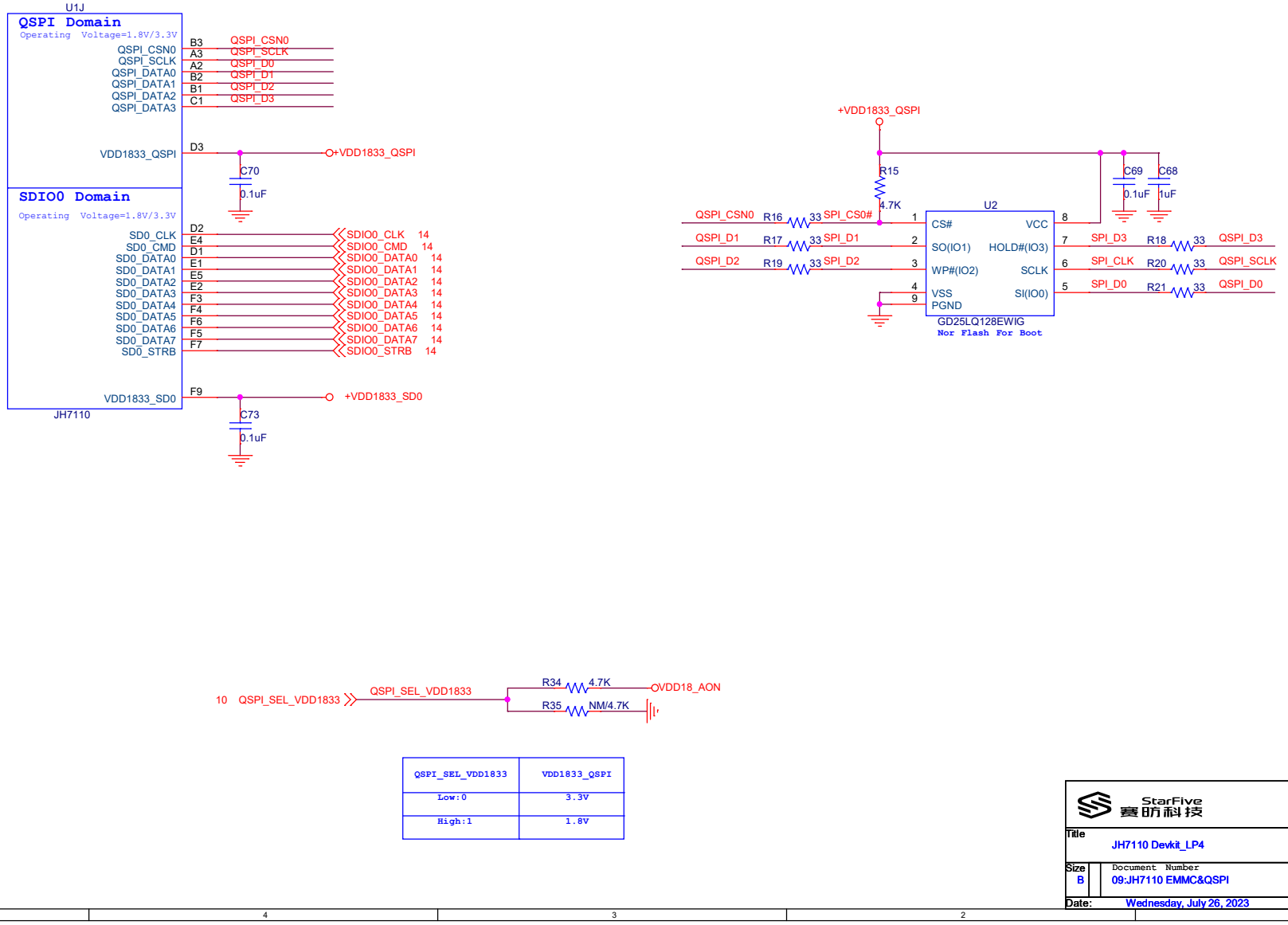
Title	JH7110 Devkit_LP4	
Size: B	Document Number: 08:JH7110 GMAC0&1	Rev: V10
Date: Wednesday, July 26, 2023	Sheet 8 of 16	



QSPI_SEL_VDD1833	VDD1833_QSPI
Low:0	3.3V
High:1	1.8V

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Title: JH7110 Devkit_LP4

Size: B | Document Number: 09:JH7110 EMMC&QSPI | Rev: V10

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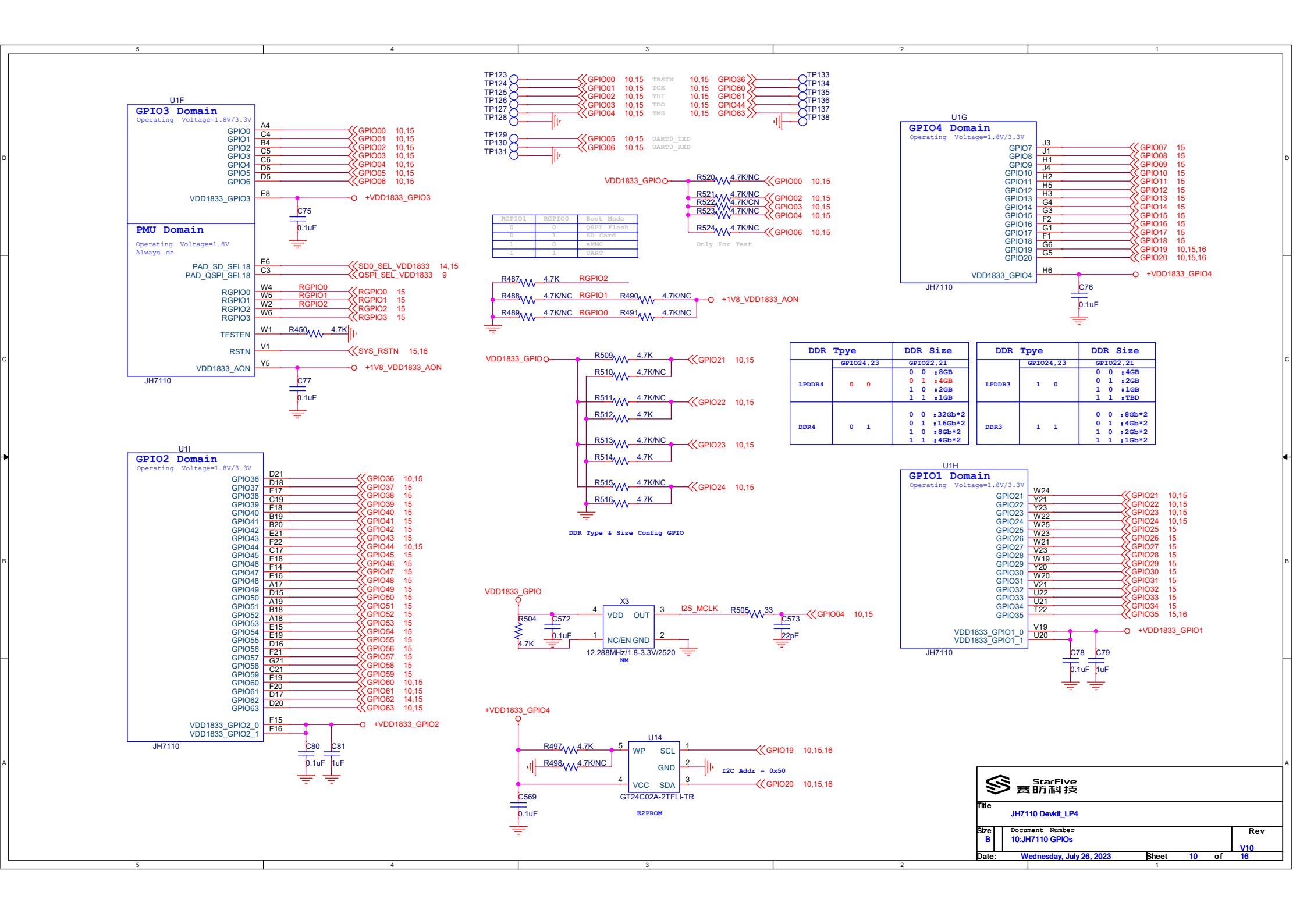
U1F
GPIO3 Domain
Operating Voltage=1.8V/3.3V
PMU Domain
Operating Voltage=1.8V
Always on
JH7110
VDD1833_GPIO3
+VDD1833_GPIO3
C75
0.1uF
PAD_SD_SEL18
PAD_QSPI_SEL18
SD0_SEL_VDD1833
QSPI_SEL_VDD1833
TESTEN
RSTN
SYS_RSTN
VDD1833_AON
+1V8_VDD1833_AON
C77
U1I
GPIO2 Domain
Operating Voltage=1.8V/3.3V
VDD1833_GPIO2_0
VDD1833_GPIO2_1
+VDD1833_GPIO2
C80
C81
1uF
TP123
TP124
TP125
TP126
TP127
TP128
TP129
TP130
TP131
TRSTN
TCK
TDI
TDO
TMS
UART0_TXD
UART0_RXD
TP133
TP134
TP135
TP136
TP137
TP138
RGPIO1
RGPIO0
Boot Mode
QSPI Flash
SD Card
eMMC
UART
Only For Test
R520
R521
R522
R523
R524
4.7K/NC
4.7K/CN
R487
R488
R489
R490
R491
RGPIO2
RGPIO1
RGPIO0
+1V8_VDD1833_AON
R509
R510
R511
R512
R513
R514
R515
R516
4.7K
4.7K/NC
DDR Type & Size Config GPIO
DDR Tpye
DDR Size
LPDDR4
LPDDR3
DDR4
DDR3
:8GB
:4GB
:2GB
:1GB
:TBD
:32Gb*2
:16Gb*2
:8Gb*2
:4Gb*2
:2Gb*2
:1Gb*2
X3
VDD OUT
NC/EN GND
12.288MHz/1.8-3.3V/2520
NM
I2S_MCLK
R504
R505
C572
C573
22pF
U14
WP SCL
GND
VCC SDA
GT24C02A-2TFLI-TR
E2PROM
I2C Addr = 0x50
C569
U1G
GPIO4 Domain
Operating Voltage=1.8V/3.3V
C76
U1H
GPIO1 Domain
Operating Voltage=1.8V/3.3V
C78
C79
StarFive
赛昉科技
Title
JH7110 Devkit_LP4
Size
B
Document Number
10:JH7110 GPIOs
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V10
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10
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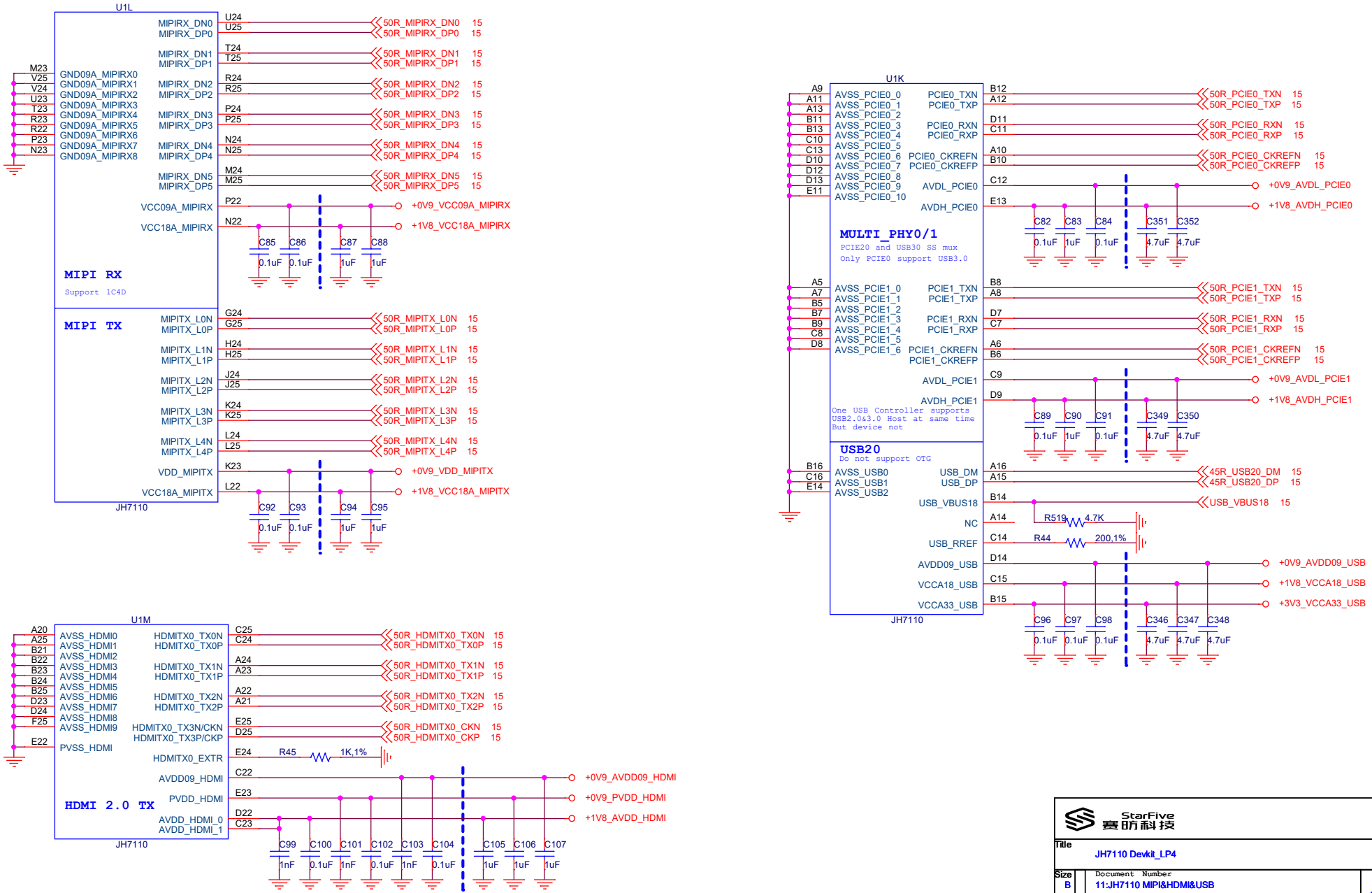
16


U1L
MIPI RX
Support 1C4D
MIPI TX
JH7110
MIPIRX_DN0
MIPIRX_DP0
MIPIRX_DN1
MIPIRX_DP1
MIPIRX_DN2
MIPIRX_DP2
MIPIRX_DN3
MIPIRX_DP3
MIPIRX_DN4
MIPIRX_DP4
MIPIRX_DN5
MIPIRX_DP5
VCC09A_MIPIRX
VCC18A_MIPIRX
GND09A_MIPIRX0
GND09A_MIPIRX1
GND09A_MIPIRX2
GND09A_MIPIRX3
GND09A_MIPIRX4
GND09A_MIPIRX5
GND09A_MIPIRX6
GND09A_MIPIRX7
GND09A_MIPIRX8
50R_MIPIRX_DN0 15
50R_MIPIRX_DP0 15
50R_MIPIRX_DN1 15
50R_MIPIRX_DP1 15
50R_MIPIRX_DN2 15
50R_MIPIRX_DP2 15
50R_MIPIRX_DN3 15
50R_MIPIRX_DP3 15
50R_MIPIRX_DN4 15
50R_MIPIRX_DP4 15
50R_MIPIRX_DN5 15
50R_MIPIRX_DP5 15
+0V9_VCC09A_MIPIRX
+1V8_VCC18A_MIPIRX
C85 C86 C87 C88
0.1uF 0.1uF 1uF 1uF
MIPITX_L0N
MIPITX_L0P
MIPITX_L1N
MIPITX_L1P
MIPITX_L2N
MIPITX_L2P
MIPITX_L3N
MIPITX_L3P
MIPITX_L4N
MIPITX_L4P
VDD_MIPITX
VCC18A_MIPITX
50R_MIPITX_L0N 15
50R_MIPITX_L0P 15
50R_MIPITX_L1N 15
50R_MIPITX_L1P 15
50R_MIPITX_L2N 15
50R_MIPITX_L2P 15
50R_MIPITX_L3N 15
50R_MIPITX_L3P 15
50R_MIPITX_L4N 15
50R_MIPITX_L4P 15
+0V9_VDD_MIPITX
+1V8_VCC18A_MIPITX
C92 C93 C94 C95
0.1uF 0.1uF 1uF 1uF
U1K
MULTI_PHY0/1
PCIE20 and USB30 SS mux
Only PCIE0 support USB3.0
USB20
Do not support OTG
One USB Controller supports
USB2.0&3.0 Host at same time
But device not
JH7110
AVSS_PCIE0_0
AVSS_PCIE0_1
AVSS_PCIE0_2
AVSS_PCIE0_3
AVSS_PCIE0_4
AVSS_PCIE0_5
AVSS_PCIE0_6
AVSS_PCIE0_7
AVSS_PCIE0_8
AVSS_PCIE0_9
AVSS_PCIE0_10
PCIE0_TXN
PCIE0_TXP
PCIE0_RXN
PCIE0_RXP
PCIE0_CKREFN
PCIE0_CKREFP
AVDL_PCIE0
AVDH_PCIE0
AVSS_PCIE1_0
AVSS_PCIE1_1
AVSS_PCIE1_2
AVSS_PCIE1_3
AVSS_PCIE1_4
AVSS_PCIE1_5
AVSS_PCIE1_6
PCIE1_TXN
PCIE1_TXP
PCIE1_RXN
PCIE1_RXP
PCIE1_CKREFN
PCIE1_CKREFP
AVDL_PCIE1
AVDH_PCIE1
AVSS_USB0
AVSS_USB1
AVSS_USB2
USB_DM
USB_DP
USB_VBUS18
NC
USB_RREF
AVDD09_USB
VCCA18_USB
VCCA33_USB
50R_PCIE0_TXN 15
50R_PCIE0_TXP 15
50R_PCIE0_RXN 15
50R_PCIE0_RXP 15
50R_PCIE0_CKREFN 15
50R_PCIE0_CKREFP 15
+0V9_AVDL_PCIE0
+1V8_AVDH_PCIE0
C82 C83 C84 C351 C352
0.1uF 1uF 0.1uF 4.7uF 4.7uF
50R_PCIE1_TXN 15
50R_PCIE1_TXP 15
50R_PCIE1_RXN 15
50R_PCIE1_RXP 15
50R_PCIE1_CKREFN 15
50R_PCIE1_CKREFP 15
+0V9_AVDL_PCIE1
+1V8_AVDH_PCIE1
C89 C90 C91 C349 C350
0.1uF 1uF 0.1uF 4.7uF 4.7uF
45R_USB20_DM 15
45R_USB20_DP 15
USB_VBUS18 15
R519 4.7K
R44 200,1%
+0V9_AVDD09_USB
+1V8_VCCA18_USB
+3V3_VCCA33_USB
C96 C97 C98 C346 C347 C348
0.1uF 0.1uF 0.1uF 4.7uF 4.7uF 4.7uF
U1M
HDMI 2.0 TX
JH7110
AVSS_HDMI0
AVSS_HDMI1
AVSS_HDMI2
AVSS_HDMI3
AVSS_HDMI4
AVSS_HDMI5
AVSS_HDMI6
AVSS_HDMI7
AVSS_HDMI8
AVSS_HDMI9
PVSS_HDMI
HDMITX0_TX0N
HDMITX0_TX0P
HDMITX0_TX1N
HDMITX0_TX1P
HDMITX0_TX2N
HDMITX0_TX2P
HDMITX0_TX3N/CKN
HDMITX0_TX3P/CKP
HDMITX0_EXTR
AVDD09_HDMI
PVDD_HDMI
AVDD_HDMI_0
AVDD_HDMI_1
50R_HDMITX0_TX0N 15
50R_HDMITX0_TX0P 15
50R_HDMITX0_TX1N 15
50R_HDMITX0_TX1P 15
50R_HDMITX0_TX2N 15
50R_HDMITX0_TX2P 15
50R_HDMITX0_CKN 15
50R_HDMITX0_CKP 15
R45 1K,1%
+0V9_AVDD09_HDMI
+0V9_PVDD_HDMI
+1V8_AVDD_HDMI
C99 C100 C101 C102 C103 C104 C105 C106 C107
1nF 0.1uF 1nF 0.1uF 1nF 0.1uF 1uF 1uF 1uF
StarFive
赛昉科技
Title
JH7110 Devkit_LP4
Size B
Document Number
11:JH7110 MIPI&HDMI&USB
Rev V10
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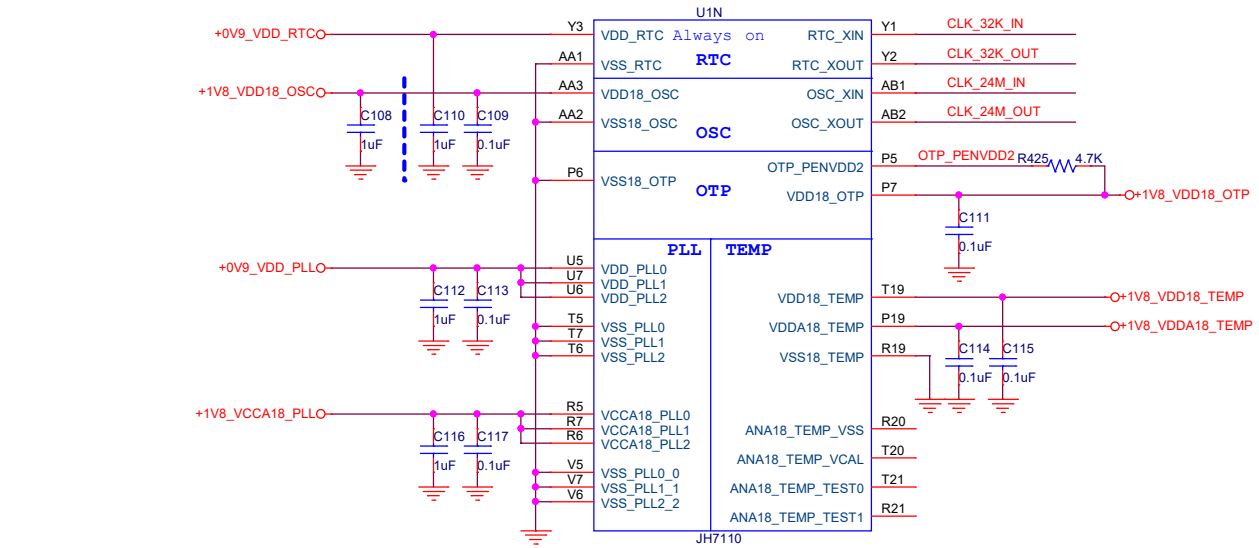

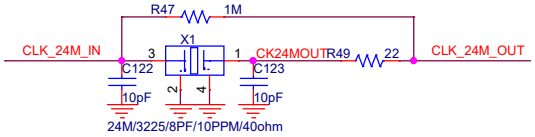

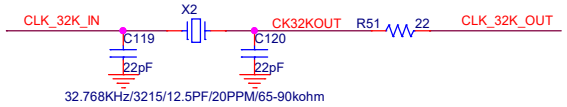

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Size B	Document Number 12:JH7110 SYS&OSC&TEMP	Rev V10
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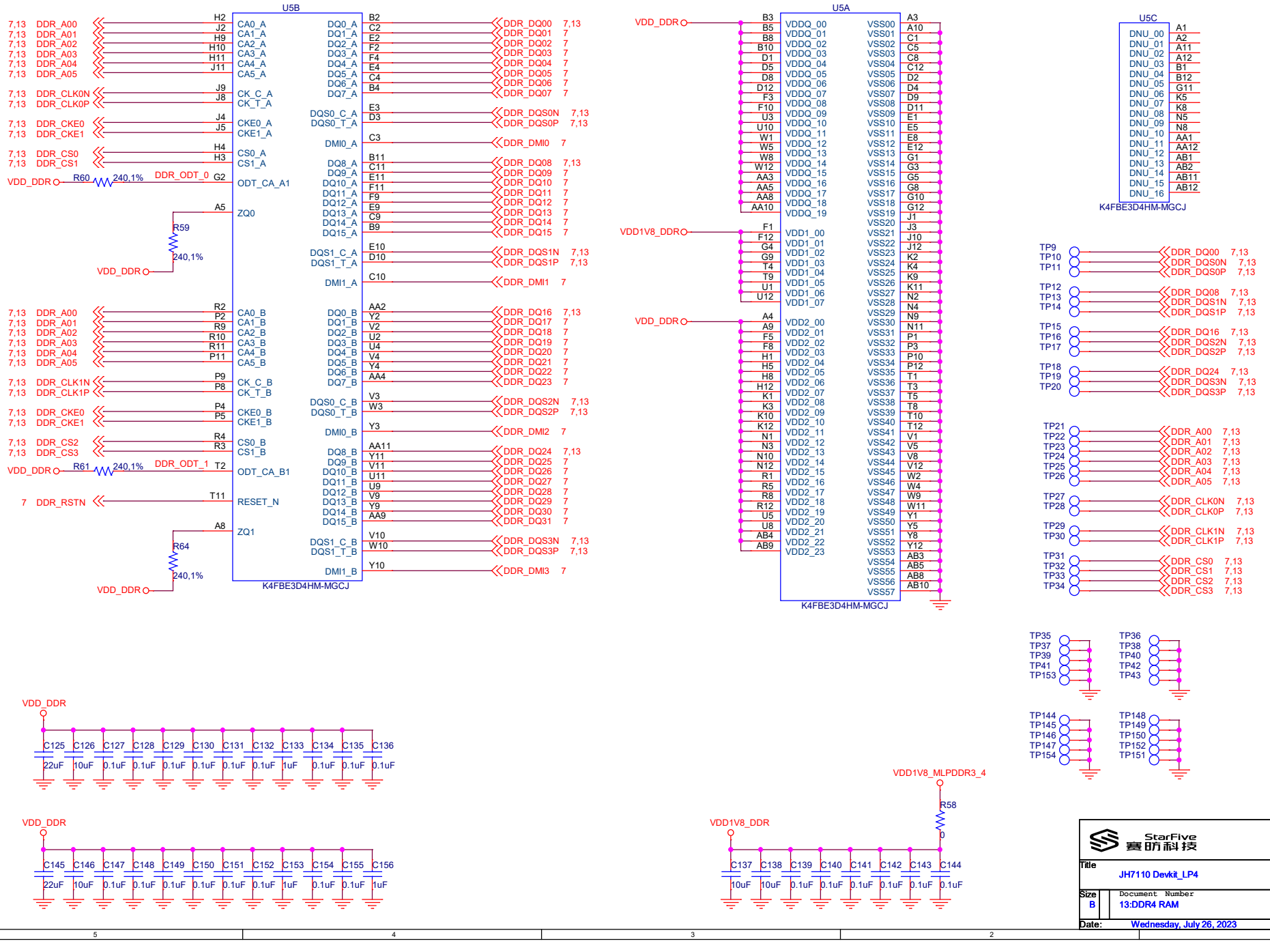
U5B
K4FBE3D4HM-MGCJ
U5A
K4FBE3D4HM-MGCJ
U5C
K4FBE3D4HM-MGCJ
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DDR_A01
DDR_A02
DDR_A03
DDR_A04
DDR_A05
DDR_CLK0N
DDR_CLK0P
DDR_CKE0
DDR_CKE1
DDR_CS0
DDR_CS1
DDR_ODT_0
DDR_ODT_1
DDR_RSTN
VDD_DDR
VDD1V8_DDR
R60
R61
R59
R64
240,1%
DDR_DQ00
DDR_DQ01
DDR_DQ02
DDR_DQ03
DDR_DQ04
DDR_DQ05
DDR_DQ06
DDR_DQ07
DDR_DQS0N
DDR_DQS0P
DDR_DMI0
DDR_DQ08
DDR_DQ09
DDR_DQ10
DDR_DQ11
DDR_DQ12
DDR_DQ13
DDR_DQ14
DDR_DQ15
DDR_DQS1N
DDR_DQS1P
DDR_DMI1
DDR_DQ16
DDR_DQ17
DDR_DQ18
DDR_DQ19
DDR_DQ20
DDR_DQ21
DDR_DQ22
DDR_DQ23
DDR_DQS2N
DDR_DQS2P
DDR_DMI2
DDR_DQ24
DDR_DQ25
DDR_DQ26
DDR_DQ27
DDR_DQ28
DDR_DQ29
DDR_DQ30
DDR_DQ31
DDR_DQS3N
DDR_DQS3P
DDR_DMI3
TP9
TP10
TP11
TP12
TP13
TP14
TP15
TP16
TP17
TP18
TP19
TP20
TP21
TP22
TP23
TP24
TP25
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TP27
TP28
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TP30
TP31
TP32
TP33
TP34
TP35
TP36
TP37
TP38
TP39
TP40
TP41
TP42
TP43
TP144
TP145
TP146
TP147
TP148
TP149
TP150
TP152
TP153
TP154
TP151
C125
C126
C127
C128
C129
C130
C131
C132
C133
C134
C135
C136
C145
C146
C147
C148
C149
C150
C151
C152
C153
C154
C155
C156
C137
C138
C139
C140
C141
C142
C143
C144
22uF
10uF
0.1uF
1uF
VDD1V8_MLPDDR3_4
R58
StarFive
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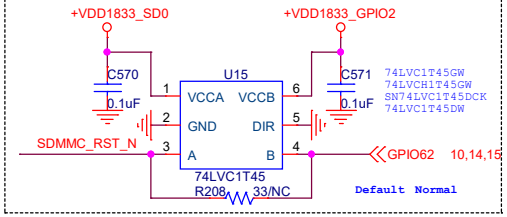
eMMC Reset Solution:

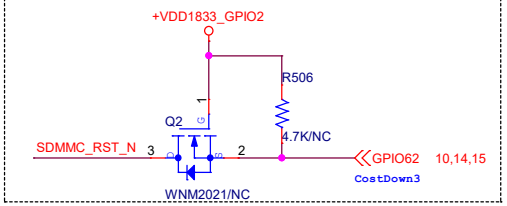
Default Normal: +VDD1833_SD0 or +VDD1833_GPIO2 = 3.3/1.8V
R196=NC;R208=NC;C234=NC;U15=ON;Q2=NC;R506=NC

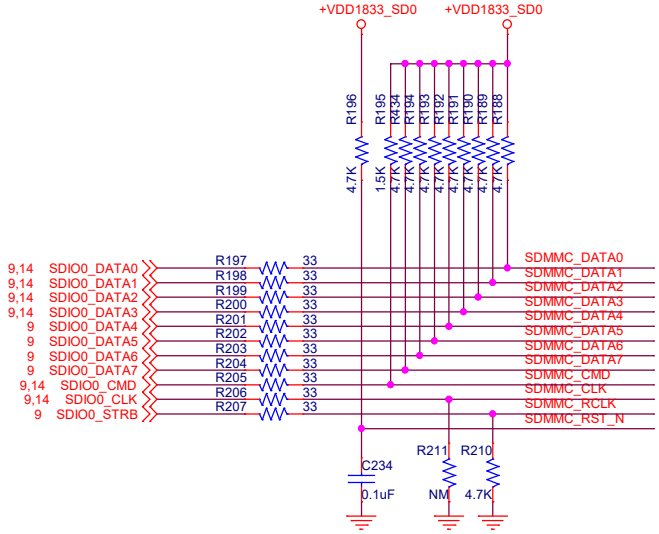
CostDown1: +VDD1833_SD0 = +VDD1833_GPIO2 = 1.8V/3.3V
R196=NC;R208=33;C234=NC;U15=NC;Q2=NC;R506=NC

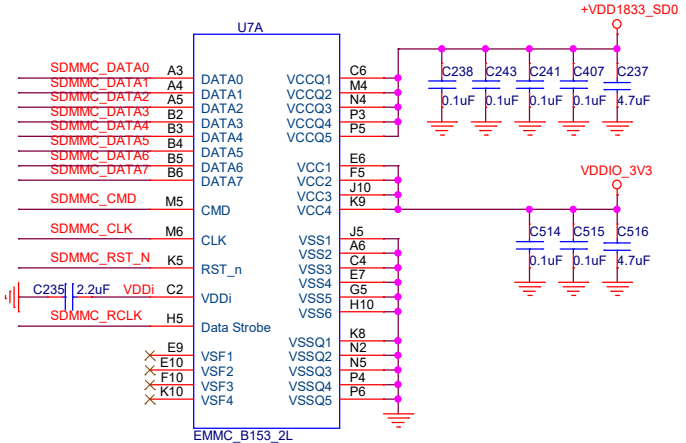
CostDown2: +VDD1833_SD0 = 1.8V & +VDD1833_GPIO2 = 3.3V
R196=NC;R208=4.7K;C234=5.6K;U15=NC;Q2=NC;R506=NC

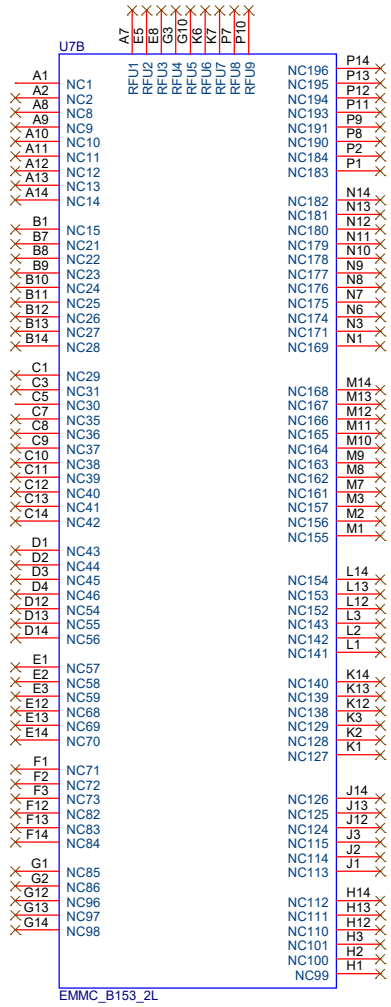
CostDown3: +VDD1833_SD0 = 3.3V & +VDD1833_GPIO2 = 1.8V
R196=4.7K;R208=NC;C234=NC;U15=NC;Q2=ON;R506=4.7K



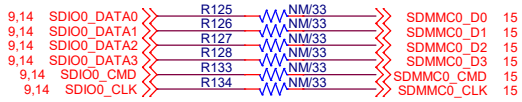


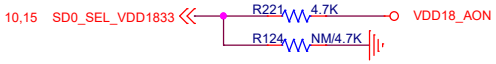






SD_SEL_VDD1833	VDD1833_SD0
Low:0	3.3V
High:1	1.8V





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Title	JH7110 Devkit_LP4	
Size B	Document Number 14:eMMC Flash	Rev V10
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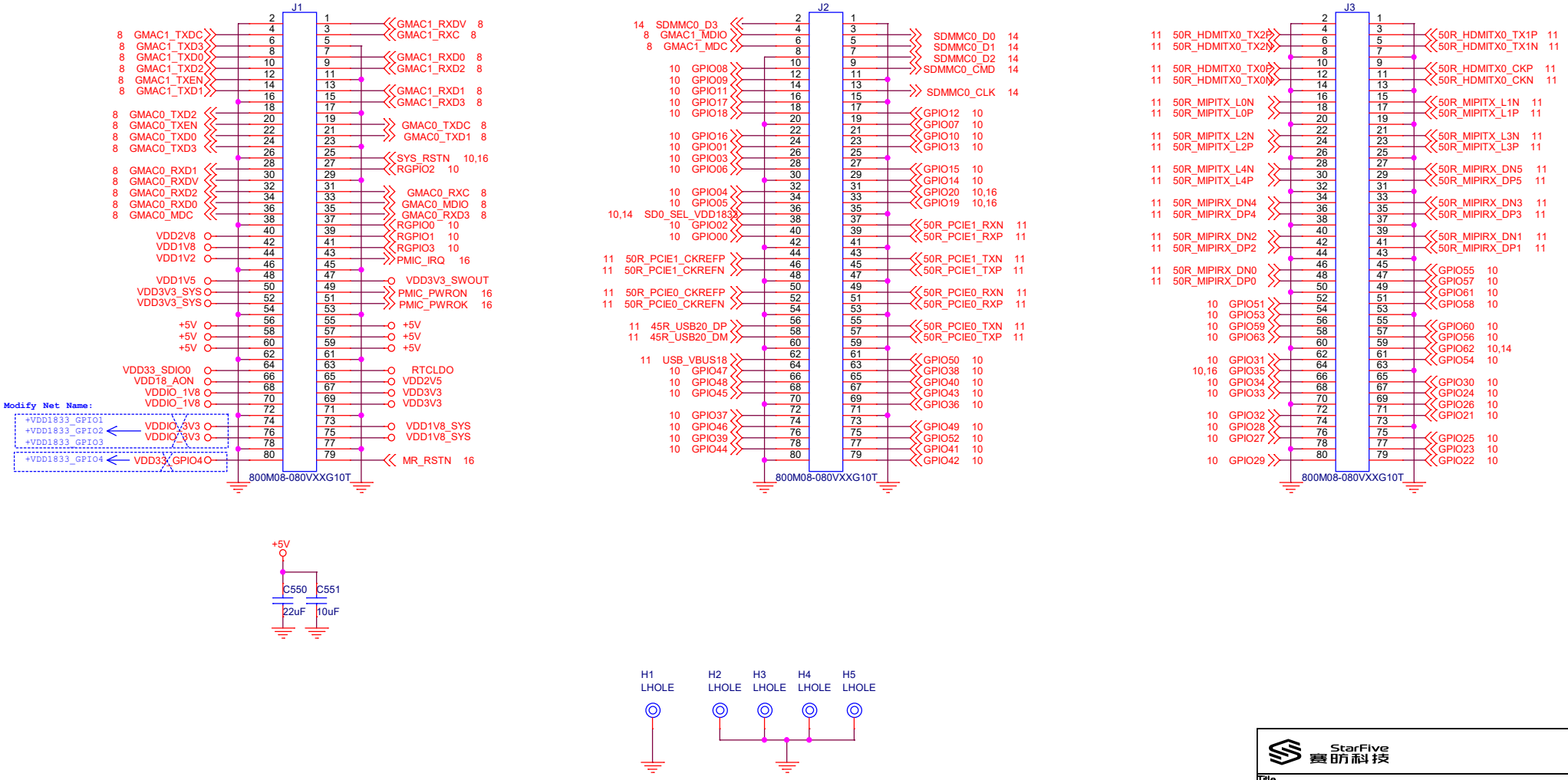

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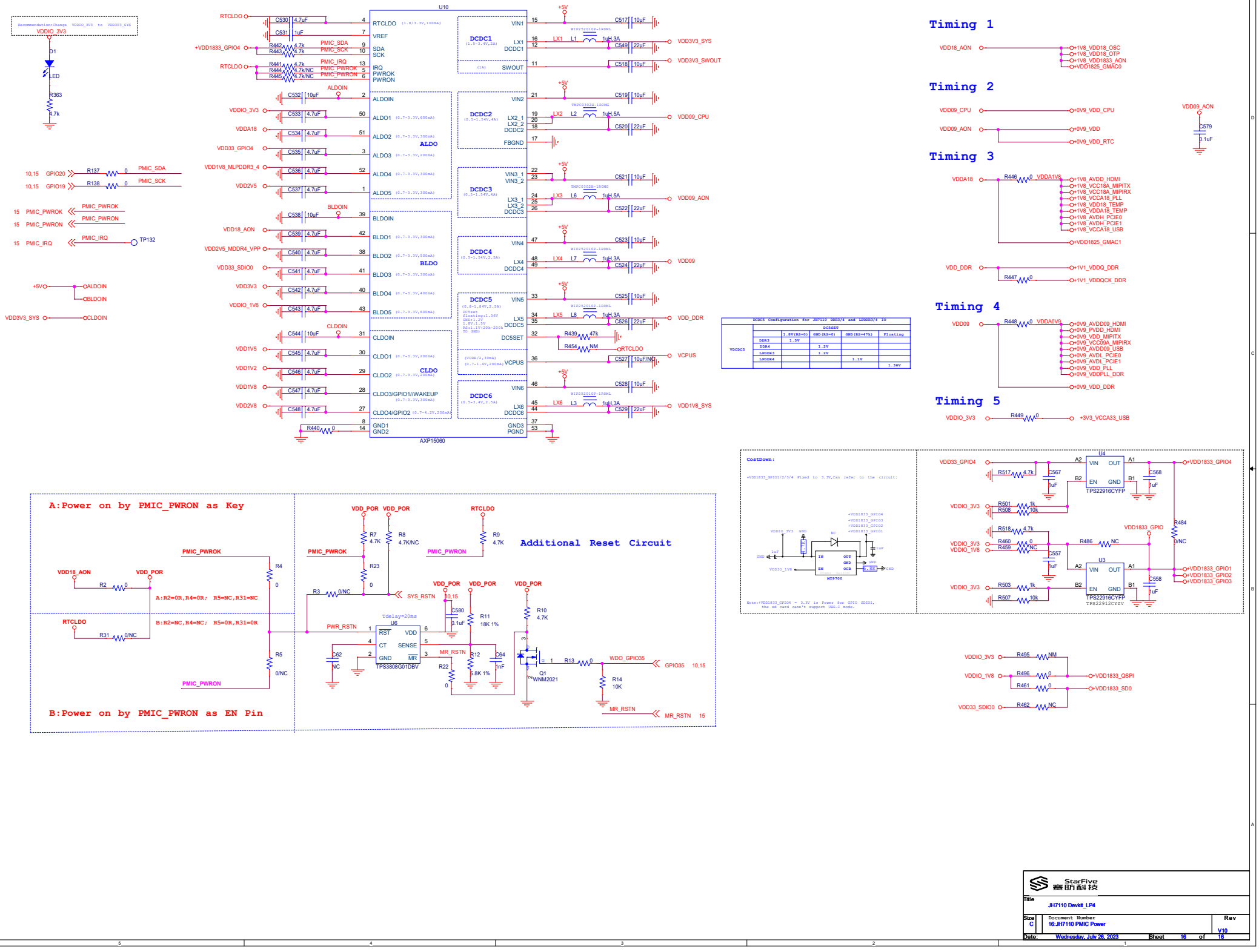
Title	JH7110 Devkit_LP4	
Size B	Document Number 15:SOM Interface	Rev V10
Date: Wednesday, July 26, 2023	Sheet 15 of 16	



DCDC5 Configuration for JH7110 DDR3/4 and LPDDR3/4 IO

	DCSSET			
VDCDC5	1.8V(RS=5)	GND(RS=0)	GND(RS=47k)	Floating
DDR3	1.5V			
DDR4		1.2V		
LPDDR3		1.2V		
LPDDR4			1.1V	
				1.36V

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Title: JH7110 Devkit_LP4

Size: C | Document Number: 16:JH7110 PMIC Power | Rev: V10

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