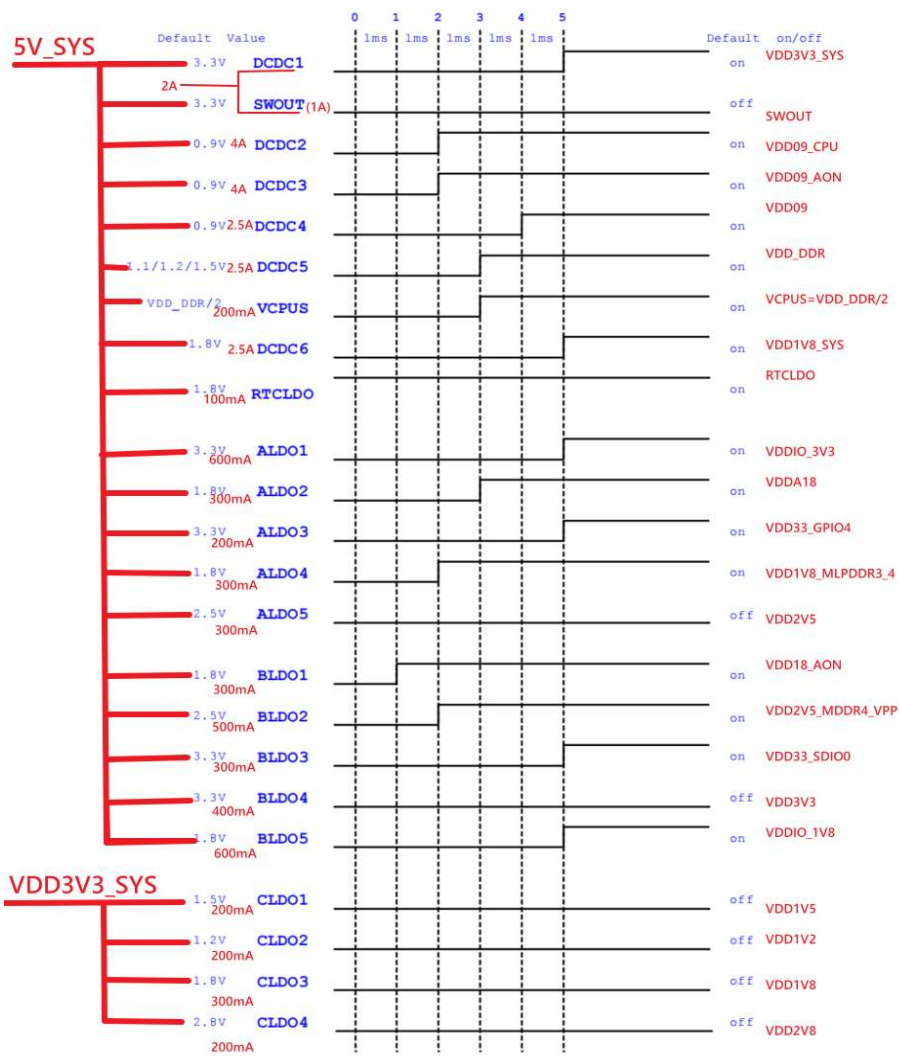
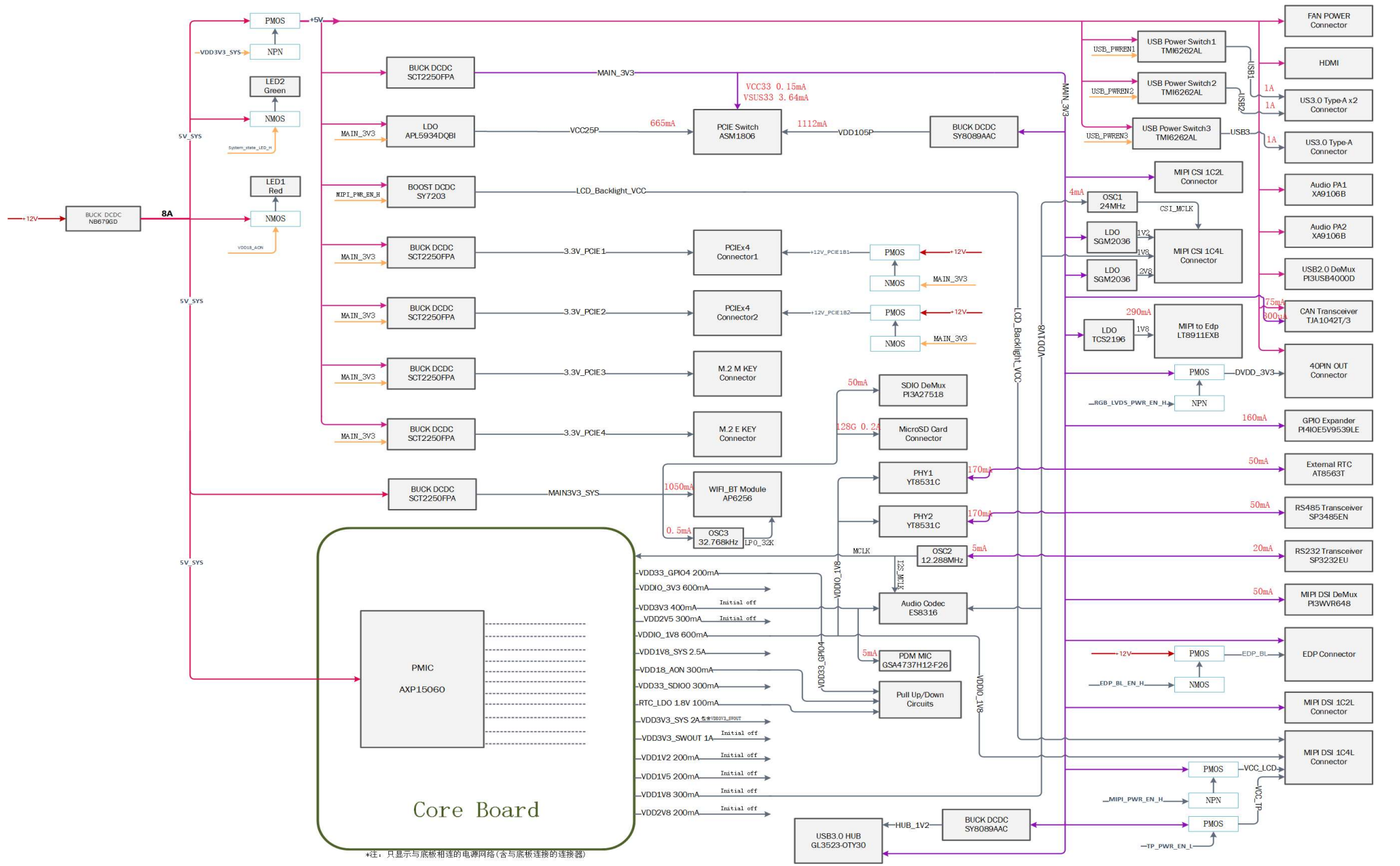


PMIC Power SEQ:





*注: 只显示与底板相连的电源网络(含与底板连接的连接器)

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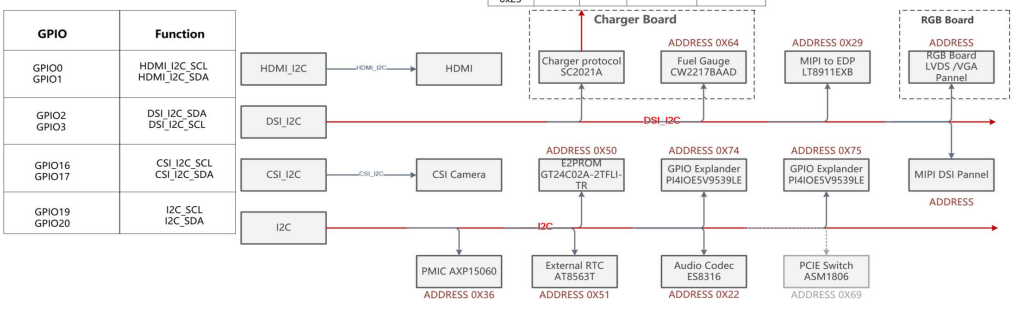
Title: JH7110_Devkit_MB_V20

Size: A3	Document Number: Power Tree	Rev: V2.0
Date: Friday, June 16, 2023	Sheet: 3 of 27	

SOC-GPIOs List		
Power Group	GPIO Name	Default FUN
VDD1833_GPIO3	GPIO00	HDMI I2C_SCL
	GPIO01	HDMI I2C_SDA
	GPIO02	DSI I2C_SDA
	GPIO03	DSI I2C_SCL
	GPIO04	I2S_MCLK
	GPIO05	UART0_TX
VDD1833_GPIO4	GPIO06	UART0_RX
	GPIO07	SD_SDI01_D2
	GPIO08	SD_SDI01_D3
	GPIO09	SD_SDI01_CMD
	GPIO10	SD_SDI01_CLK
	GPIO11	SD_SDI01_D0
	GPIO12	SD_SDI01_D1
	GPIO13	PCIE1A_PFSN / PCIE1B_CLKREQ
	GPIO14	HDMI_CEC
	GPIO15	HDMI_HPD
	GPIO16	CSI_I2C_SCL
	GPIO17	CSI_I2C_SDA
	GPIO18	PCIE1A_PERST# / PCIE1B_PERST#
	GPIO19	I2C_SCL
GPIO20	I2C_SDA	
VDD1833_GPIO1	GPIO21	DDR_CONFIG1_DDR_capacity_size
	GPIO22	DDR_CONFIG2_DDR_capacity_size
	GPIO23	DDR_CONFIG3_DDR_Category
	GPIO24	DDR_CONFIG4_DDR_Category
	GPIO25	CAN0_TXD
	GPIO26	CAN0_RXD
	GPIO27	FAN_PWM
	GPIO28	CAN0_STBY
	GPIO29	SD_SDI01_CD
	GPIO30	GPIO_EXP_INT
	GPIO31	TP_INT
	GPIO32	UART_TXD_485
	GPIO33	MIPI_EDP_PWM/GPIO33 --> J5(R6)
	GPIO34	UART_RXD_485
	GPIO35	WDO_RST
VDD1833_GPIO2	GPIO36	GPIO36 --> J5(RGB_CLK)
	GPIO37	GPIO37 --> J5(VSYNC)
	GPIO38	I2S_SCLK/GPIO38-->J5(HSYNC)
	GPIO39	PA_EN_H/GPIO39 --> J5(DE)
	GPIO40	GPIO40 --> J5(B0)
	GPIO41	LT8911EXB_RST/GPIO41--> J5(B1)
	GPIO42	GPIO42 --> J5(B2)
	GPIO43	GPIO43 --> J5(B3)
	GPIO44	I2S_DSDIN/GPIO44-->J5(B4)
	GPIO45	UART_TXD_232/GPIO45-->J5(B5)
	GPIO46	UART_RXD_232/GPIO46-->J5(B6)
	GPIO47	GPIO47 --> J5(B7)
	GPIO48	GPIO48 --> J5(B0)
	GPIO49	GPIO49 --> J5(G1)
	GPIO50	GPIO50 --> J5(G2)
	GPIO51	GPIO51 --> J5(G3)
	GPIO52	BT_EN_H/GPIO52 --> J5(G4)
	GPIO53	BT_UART_TXD/GPIO53 --> J5(G5)
	GPIO54	BT_UART_RXD/GPIO54 --> J5(G6)
	GPIO55	BT_UART_RTS/GPIO55 --> J5(G7)
	GPIO56	BT_UART_CTS/GPIO56 --> J5(R0)
	GPIO57	GPIO57 --> J5(R1)
	GPIO58	GPIO58 --> J5(R2)
GPIO59	GPIO59 --> J5(R3)	
GPIO60	GPIO60 --> J5(R4)	
GPIO61	I2S_ASDOUT/GPIO61 --> J5(R5)	
GPIO62	SDI00_RSTN	
GPIO63	I2S_LRCK/GPIO63 --> J5(R7)	
VDD18_AON	RGPIO0	Boot Mode
	RGPIO1	Boot Mode
	RGPIO2	Boot Mode

9539 Expand-GPIOs List		
9539_GPIO	Function	
	GPIO Expander1 U24	GPIO Expander2 U50
P0_0	PCIE1_PWREN_H	1806_PWR_EN1
P0_1	WIFI_EN_H	1806_PWR_EN2
P0_2	System_state_LED_H	PCIE1B1_PWR_EN
P0_3	RGB_LVDS_PWR_EN_H	PCIE1B1_PFSN
P0_4	MIPI_PWR_EN_H	PCIE1B2_PFSN
P0_5	MIPI_SEL_H	PCIE1B3_PWR_EN
P0_6	EDP_BL_EN_H	PCIE1B4_PWR_EN
P0_7	SDI01_SEL_H	485_CTR
P1_0	TP_RST_L	RTC_INT#
P1_1	TP_PWR_EN_L	BT_DIS_N
P1_2	CSI_RST_L	WL_DIS_N
P1_3	CSI_PWDN_L	HUB_RST_L
P1_4	LCD_RESET_L	FAN_SPEED
P1_5	HP_IRQ	EXGPIO1
P1_6	INT_SC2021	EXGPIO2
P1_7	BT_WAKE	EXGPIO3

SC2021A Addr	I2C		Firmware	
	Write	Read	Write	Read
0x00-0x0F	Available	Available	NA	Available
0x10-0x1F	NA	Available	Available	Available
0x20-0x23	Available	Available	Available	Available

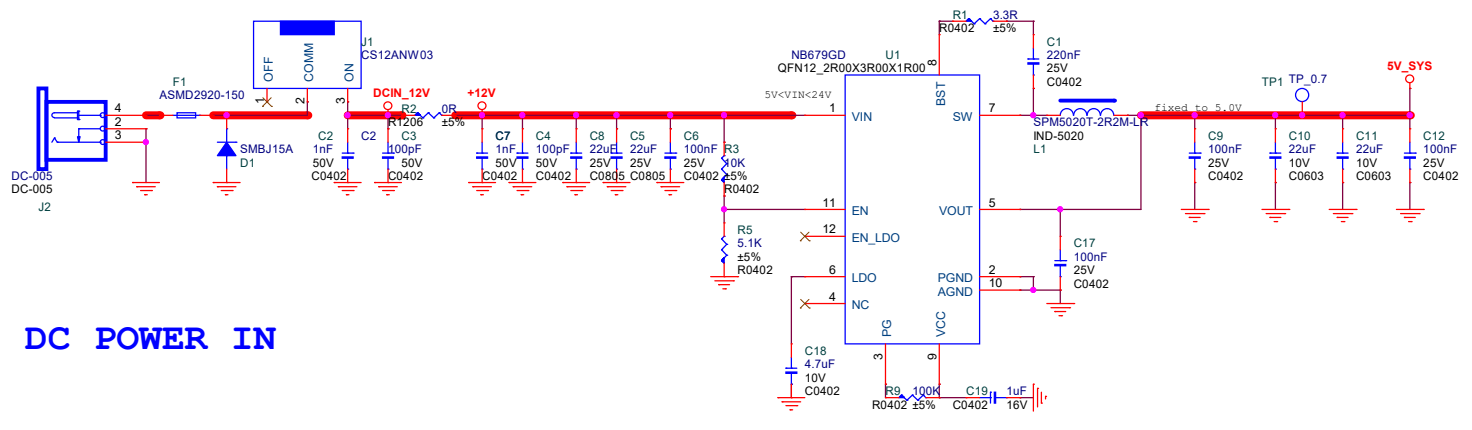


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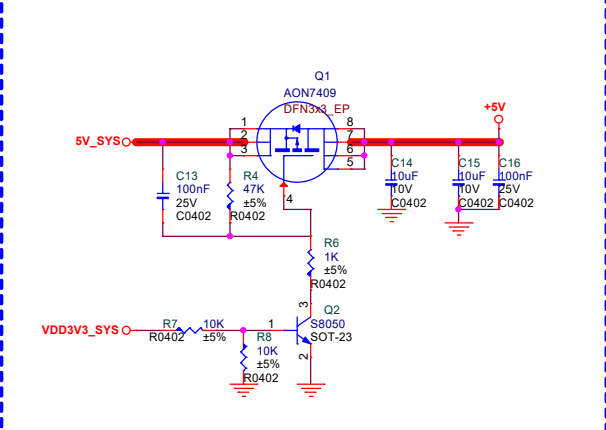
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Title: JH7110_Devkit_MB_V20

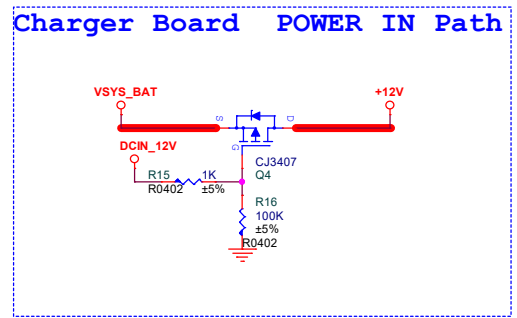
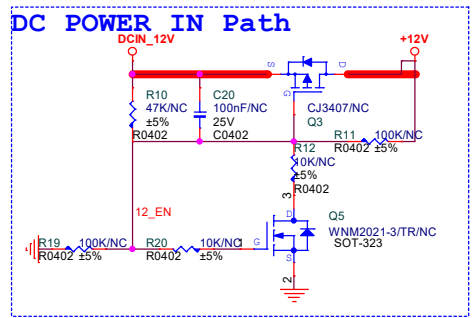
Size: A3	Document Number: GPIO Lists & I2C Addresses	Rev: V2.0
Date: Friday, June 16, 2023	Sheet: 4	of: 27



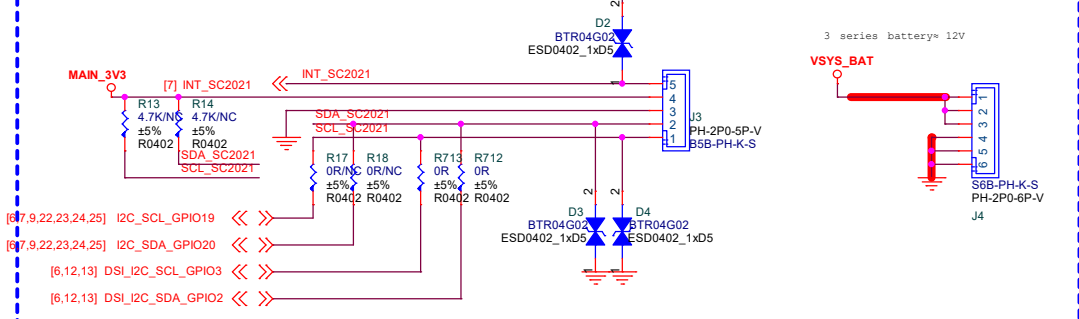
DC POWER IN



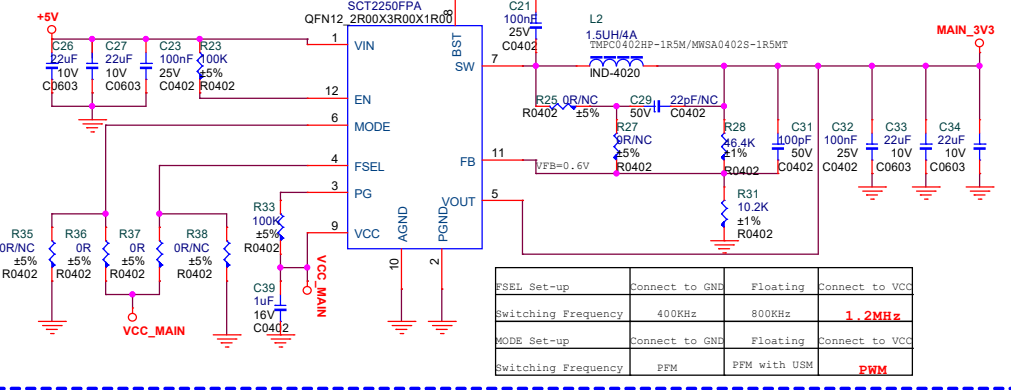
Power Path Management



Connect Charger Board

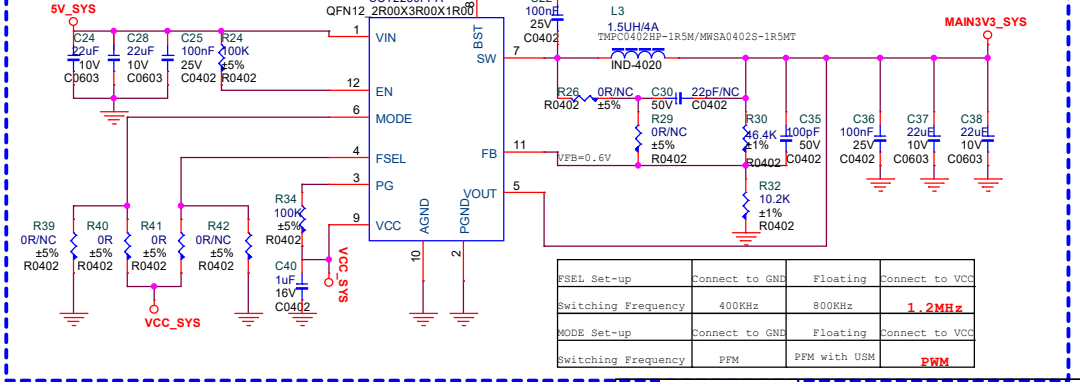


MAIN3V3



FSEL Set-up	Connect to GND	Floating	Connect to VCC
Switching Frequency	400KHz	800KHz	1.2MHz
MODE Set-up	Connect to GND	Floating	Connect to VCC
Switching Frequency	PFM	PFM with USM	PWM

MAIN3V3_SYS



FSEL Set-up	Connect to GND	Floating	Connect to VCC
Switching Frequency	400KHz	800KHz	1.2MHz
MODE Set-up	Connect to GND	Floating	Connect to VCC
Switching Frequency	PFM	PFM with USM	PWM



SOM Interface

RGPIO

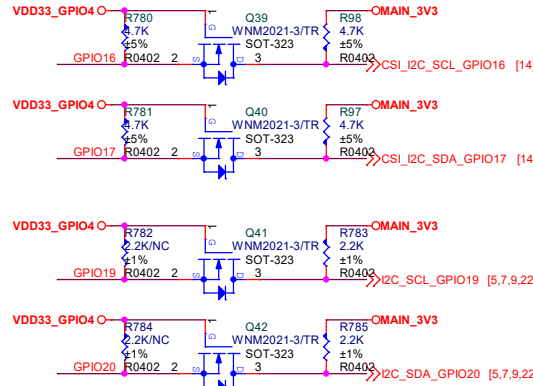
RGPI00 R0402 R42 0R ±5% >> BOOT_Mode_RGPI00 [7]
 RGPI01 R0402 R42 0R ±5% >> BOOT_Mode_RGPI01 [7]
 RGPI02 R0402 R42 0R ±5% >> BOOT_Mode_RGPI02 [7]
 RGPI03 R0402 R42 0R ±5% >> System_Wake_RGPI03 [9]

GPIO3 Domain

GPIO00 >> HDMI_I2C_SCL_GPIO0 [15]
 GPIO01 >> HDMI_I2C_SDA_GPIO1 [15]
 GPIO02 >> DSI_I2C_SDA_GPIO2 [5,12,13]
 GPIO03 >> DSI_I2C_SCL_GPIO3 [5,12,13]
 GPIO04 >> I2S_MCLK_GPIO4 [25]
 GPIO05 >> UART0_TX_GPIO5 [20]
 GPIO06 >> UART0_RX_GPIO6 [20]

GPIO4 Domain

GPIO07 >> SD_SDI01_D2_GPIO7 [11]
 GPIO08 >> SD_SDI01_D3_GPIO8 [11]
 GPIO09 >> SD_SDI01_CMD_GPIO9 [11]
 GPIO10 >> SD_SDI01_CLK_GPIO10 [11]
 GPIO11 >> SD_SDI01_D0_GPIO11 [11]
 GPIO12 >> SD_SDI01_D1_GPIO12 [11]
 GPIO13 >> GPIO13 [6,21]
 GPIO14 >> HDMI_CEC_GPIO14 [15]
 GPIO15 >> HDMI_HPD_GPIO15 [15]
 GPIO16 >> GPIO16 [6,21]
 GPIO17 >> GPIO17 [6,21]
 GPIO18 >> GPIO18 [6,21]
 GPIO19 >> GPIO19 [6,21]
 GPIO20 >> GPIO20 [6,21]

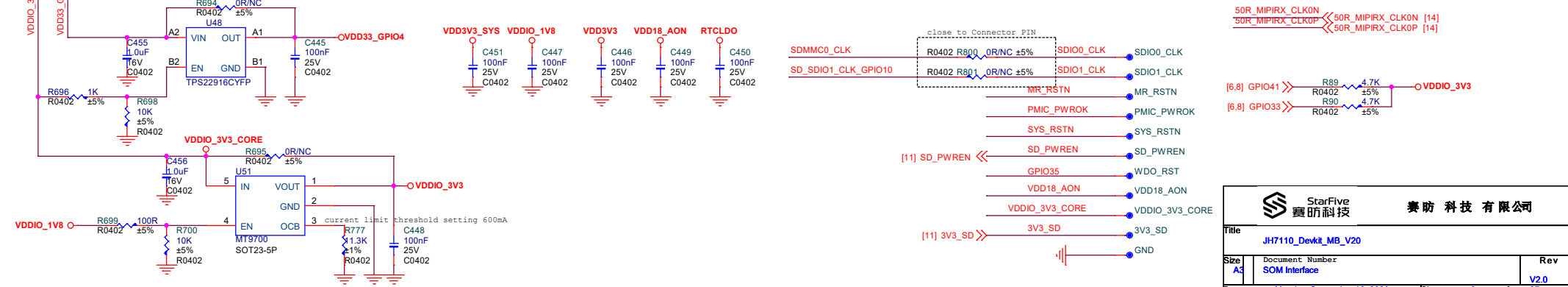
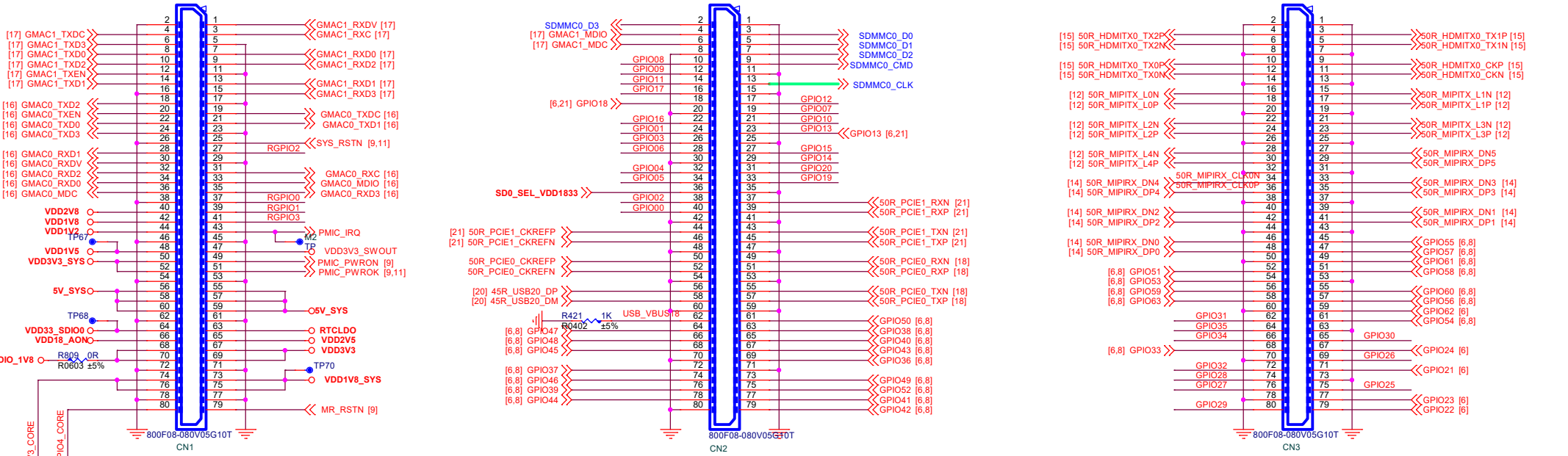


GPIO1 Domain

GPIO21 >> GPIO21 [6] DDR capacity size
 GPIO22 >> GPIO22 [6] DDR Category
 GPIO23 >> CAN0_TXD [10]
 GPIO24 >> CAN0_RXD [10]
 GPIO25 >> CAN0_TXD [10]
 GPIO26 >> CAN0_RXD [10]
 GPIO27 >> FAN_PWM_GPIO27 [9]
 GPIO28 >> CAN0_STBY [10]
 GPIO29 >> SD_SDI01_CD_GPIO29 [11]
 GPIO30 >> GPIO_EXP_INT [7]
 GPIO31 >> TP_INT_GPIO31 [12]
 GPIO32 >> UART_TXD_485 [10]
 GPIO33 >> GPIO33 [6,8]
 GPIO34 >> UART_RXD_485 [10]

GPIO2 Domain

GPIO36 >> GPIO36 [6,8]
 GPIO37 >> GPIO37 [6,8]
 GPIO38 >> GPIO38 [6,8]
 GPIO39 >> GPIO39 [6,8]
 GPIO40 >> GPIO40 [6,8]
 GPIO41 >> GPIO41 [6,8]
 GPIO42 >> GPIO42 [6,8]
 GPIO43 >> GPIO43 [6,8]
 GPIO44 >> GPIO44 [6,8]
 GPIO45 >> GPIO45 [6,8]
 GPIO46 >> GPIO46 [6,8]
 GPIO47 >> GPIO47 [6,8]
 GPIO48 >> GPIO48 [6,8]
 GPIO49 >> GPIO49 [6,8]
 GPIO50 >> GPIO50 [6,8]
 GPIO51 >> GPIO51 [6,8]
 GPIO52 >> GPIO52 [6,8]
 GPIO53 >> GPIO53 [6,8]
 GPIO54 >> GPIO54 [6,8]
 GPIO55 >> GPIO55 [6,8]
 GPIO56 >> GPIO56 [6,8]
 GPIO57 >> GPIO57 [6,8]
 GPIO58 >> GPIO58 [6,8]
 GPIO59 >> GPIO59 [6,8]
 GPIO60 >> GPIO60 [6,8]
 GPIO61 >> GPIO61 [6,8]
 GPIO62 >> GPIO62 [6,8]
 GPIO63 >> GPIO63 [6,8]

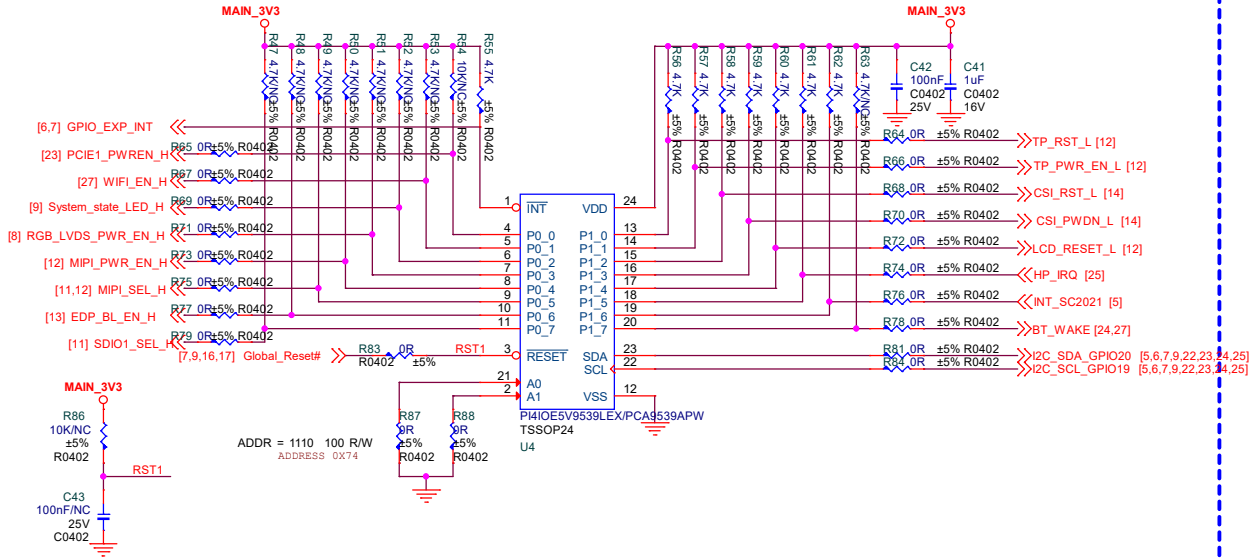


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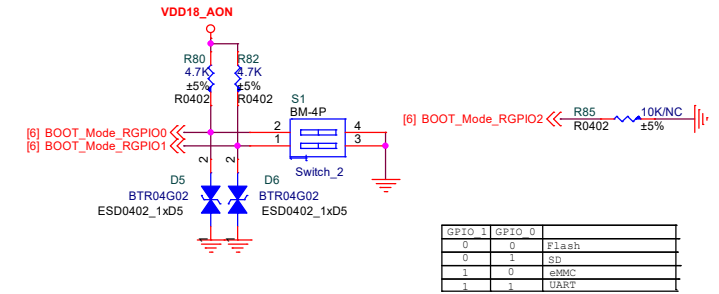
Title JH7110_Devkit_MB_V20		
Size A4	Document Number SOM Interface	Rev V2.0
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GPIO Expander1



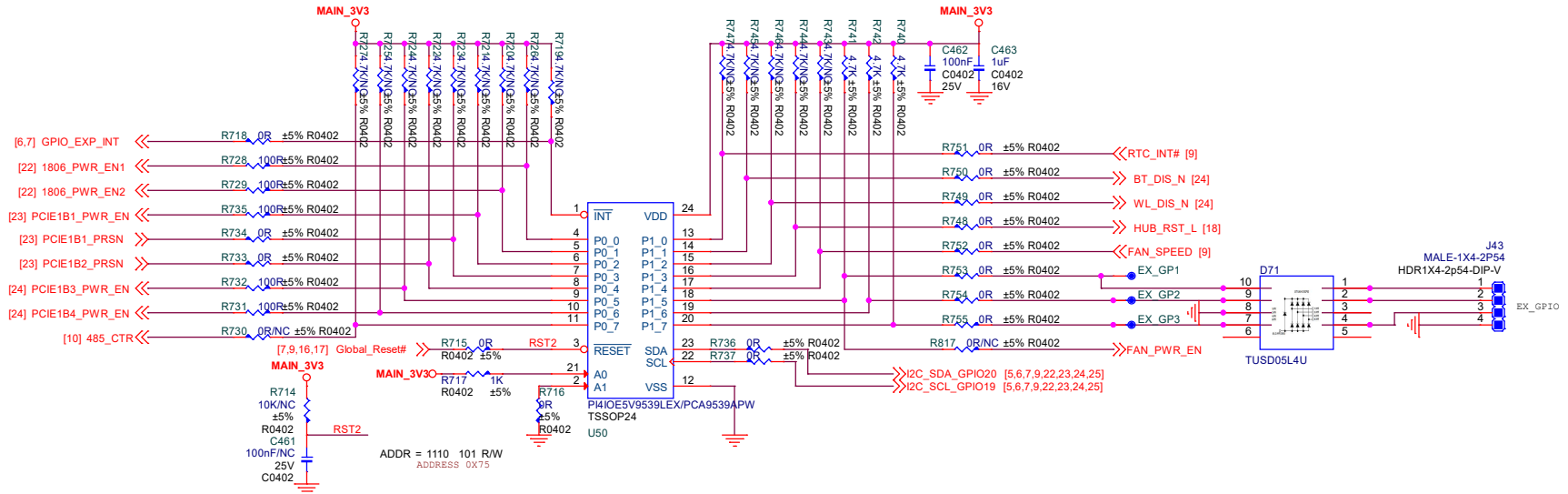
BOOT MODE


BOOT MODE (RGP102)	Boot Vector	Boot Selection (RGP101,0)	Note
0x1	0x00_2100_0000	XIP Flash	can not boot from XIP Flash, if disabled thru OTP Configuration.
0x0	0x00_2A00_0000	0x0: 1Bit QSPI Nor Flash 0x1: SDIO3.0 0x2: eMMC5.0 0x3: UART	on-chip boot ROM (32KB)



GPIO 1	GPIO 0	
0	0	Flash
0	1	SD
1	0	eMMC
1	1	UART

GPIO Expander2



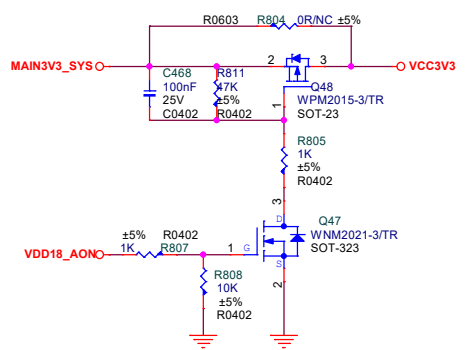
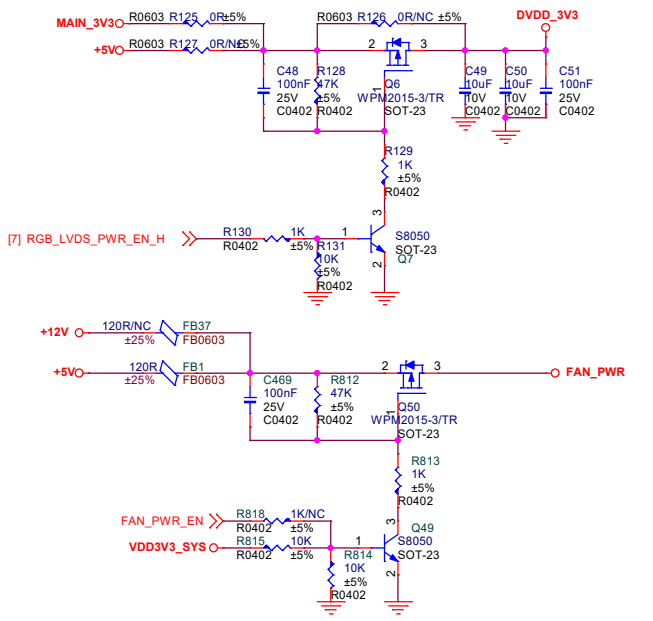
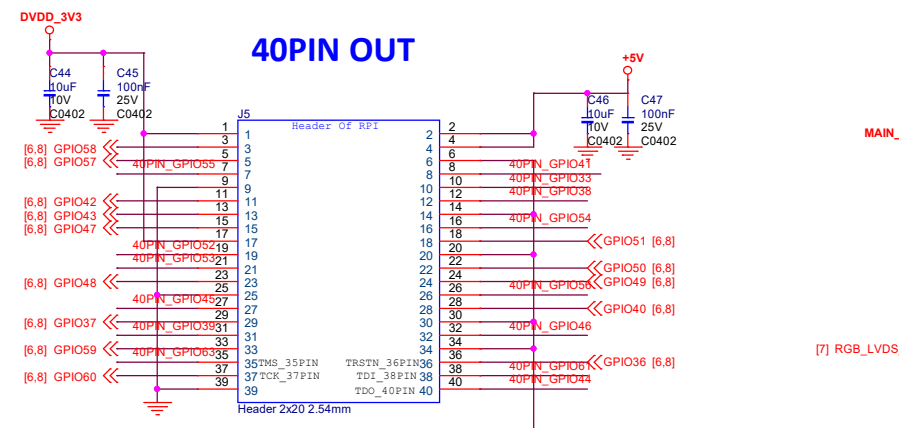
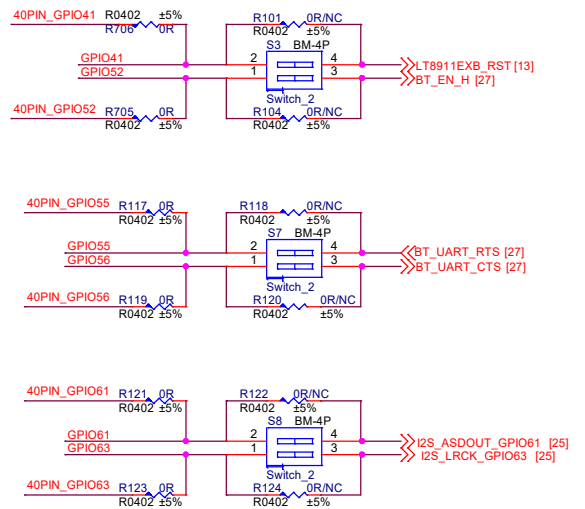
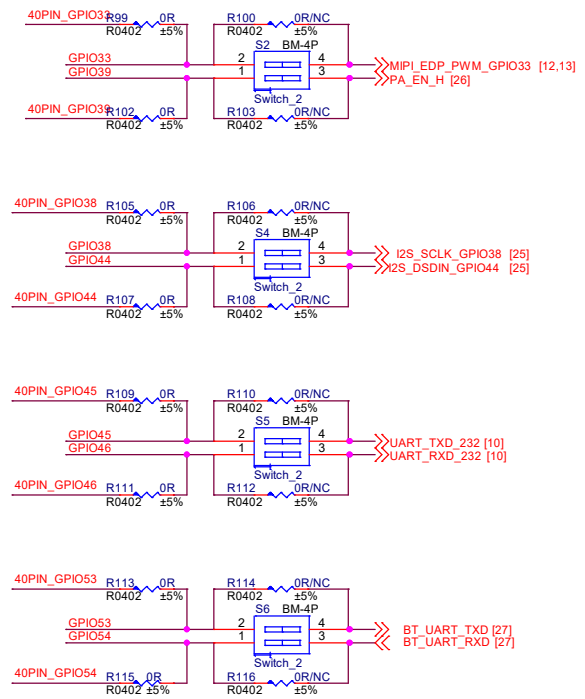

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Title: JH7110_DevKit_MB_V20
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 Date: Monday, September 18, 2023 Sheet 7 of 27

[6.8]	GPIO36	GPIO36	LCD_CLK	LCD_CLK	RGB_CLK	
[6.8]	GPIO37	GPIO37	LCD_VSYNC	LCD_VSYNC	VSYNC	
[6.8]	GPIO38	GPIO38	LCD_HSYNC	LCD_HSYNC	HSYNC	
[6.8]	GPIO39	GPIO39	LCD_DE	LCD_DE	RGB_DE	
[6.8]	GPIO40	GPIO40	DATA0	DATA0	B0	DATA0
[6.8]	GPIO41	GPIO41	DATA1	DATA1	B1	
[6.8]	GPIO42	GPIO42	DATA2	DATA2	B2	
[6.8]	GPIO43	GPIO43	DATA3	DATA3	B3	
[6.8]	GPIO44	GPIO44	DATA4	DATA4	B4	
[6.8]	GPIO45	GPIO45	DATA5	DATA5	B5	
[6.8]	GPIO46	GPIO46	DATA6	DATA6	B6	
[6.8]	GPIO47	GPIO47	DATA7	DATA7	B7	
[6.8]	GPIO48	GPIO48	DATA8	DATA8	G0	
[6.8]	GPIO49	GPIO49	DATA9	DATA9	G1	
[6.8]	GPIO50	GPIO50	DATA10	DATA10	G2	
[6.8]	GPIO51	GPIO51	DATA11	DATA11	G3	
[6.8]	GPIO52	GPIO52	DATA12	DATA12	G4	
[6.8]	GPIO53	GPIO53	DATA13	DATA13	G5	
[6.8]	GPIO54	GPIO54	DATA14	DATA14	G6	
[6.8]	GPIO55	GPIO55	DATA15	DATA15	G7	
[6.8]	GPIO56	GPIO56	DATA16	DATA16	R0	
[6.8]	GPIO57	GPIO57	DATA17	DATA17	R1	
[6.8]	GPIO58	GPIO58	DATA18	DATA18	R2	
[6.8]	GPIO59	GPIO59	DATA19	DATA19	R3	
[6.8]	GPIO60	GPIO60	DATA20	DATA20	R4	
[6.8]	GPIO61	GPIO61	DATA21	DATA21	R5	
[6.8]	GPIO62	GPIO62	DATA22	DATA22	R6	
[6.8]	GPIO63	GPIO63	DATA23	DATA23	R7	

RGB888

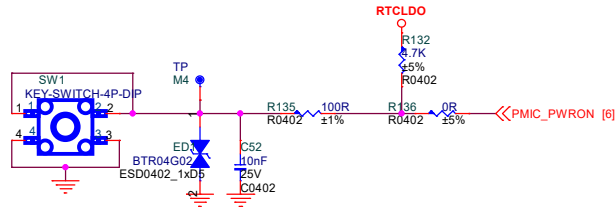



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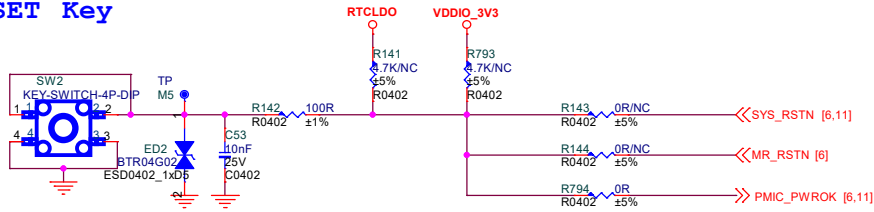
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 Size: A3
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PWRON Key

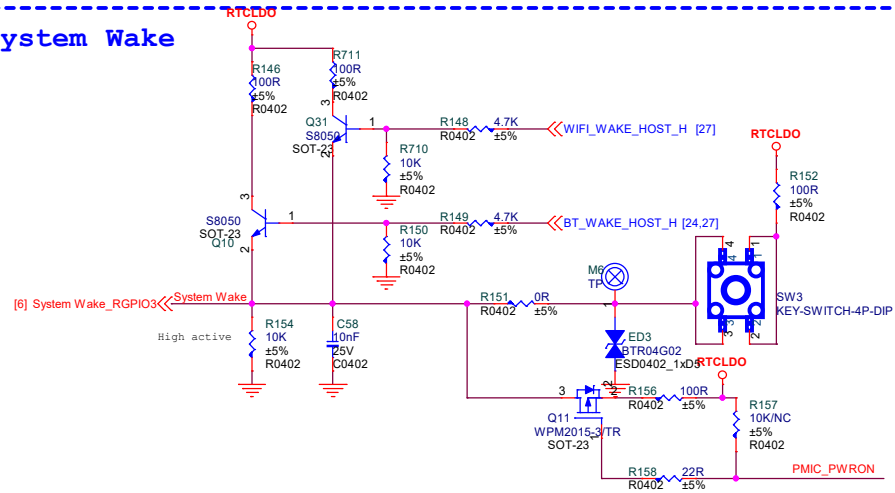
*长按 6 s 关机, 短 按1 s 开机



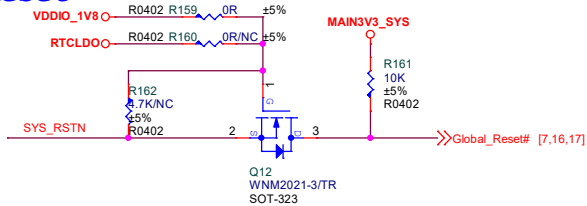
RESET Key



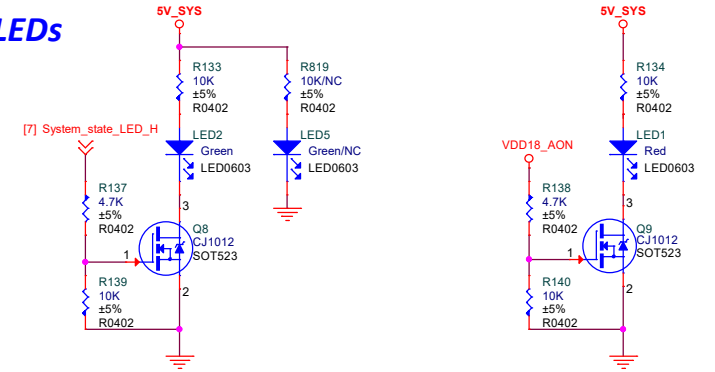
System Wake



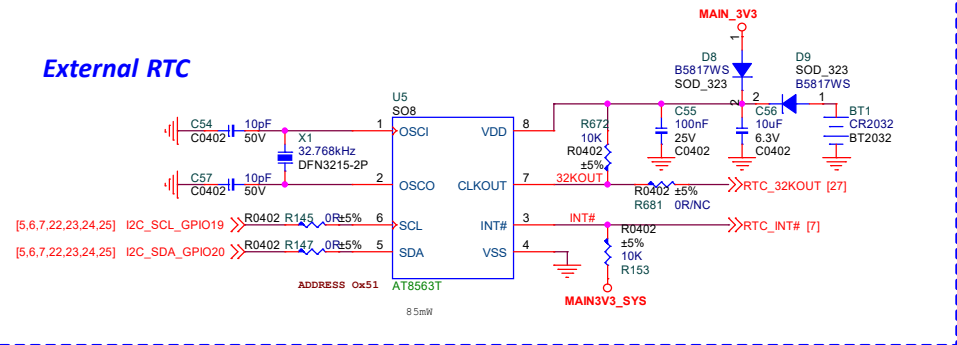
Global Reset



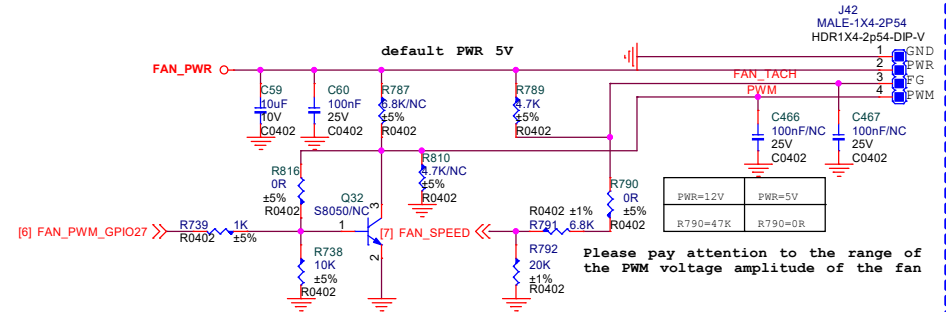
ACK&Power LEDs



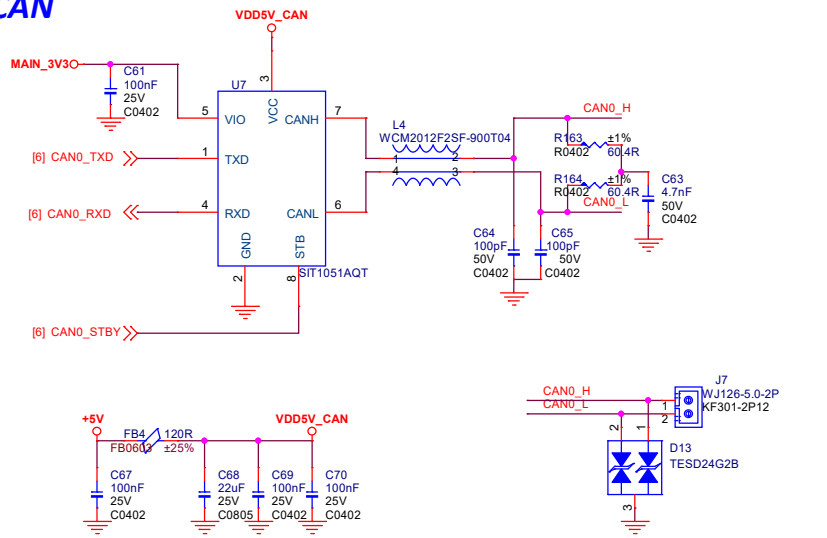
External RTC



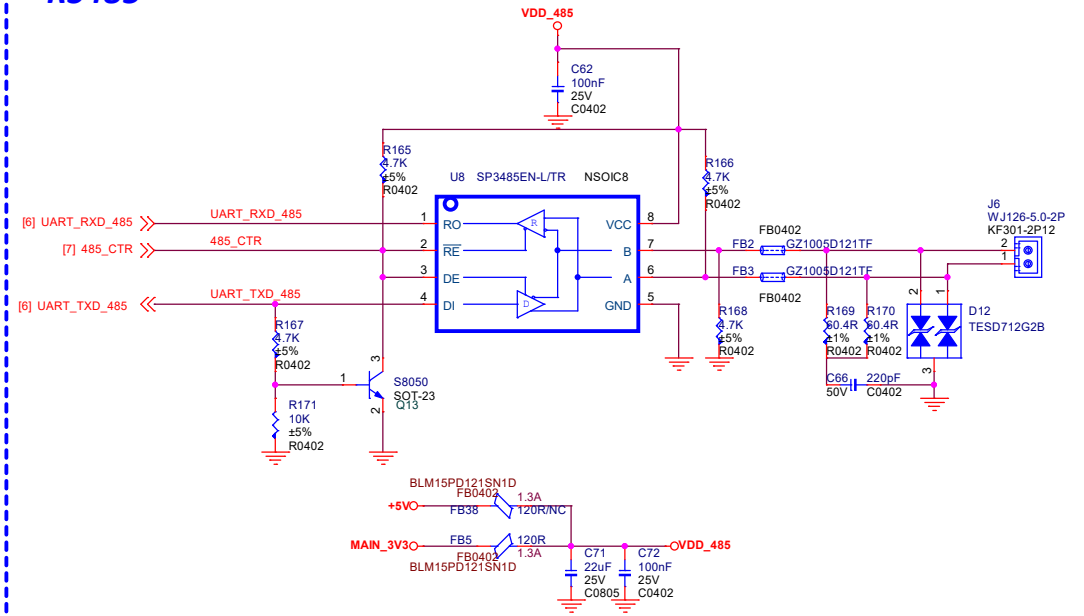
FAN Circuit



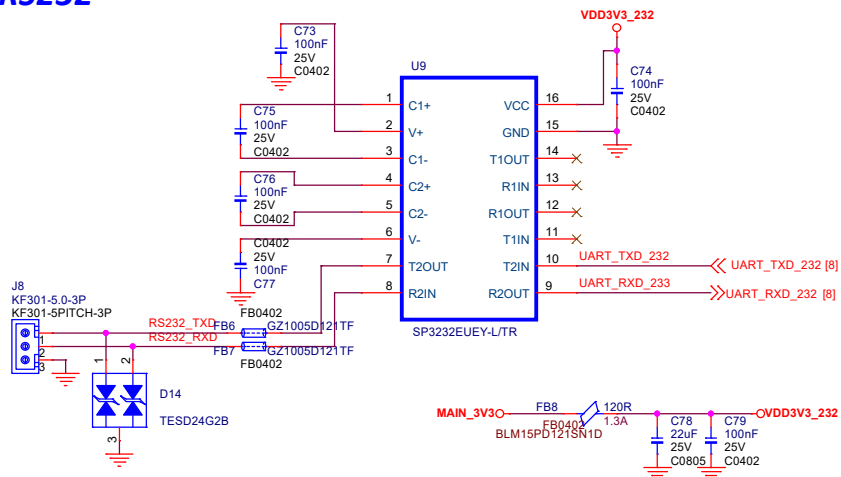
CAN



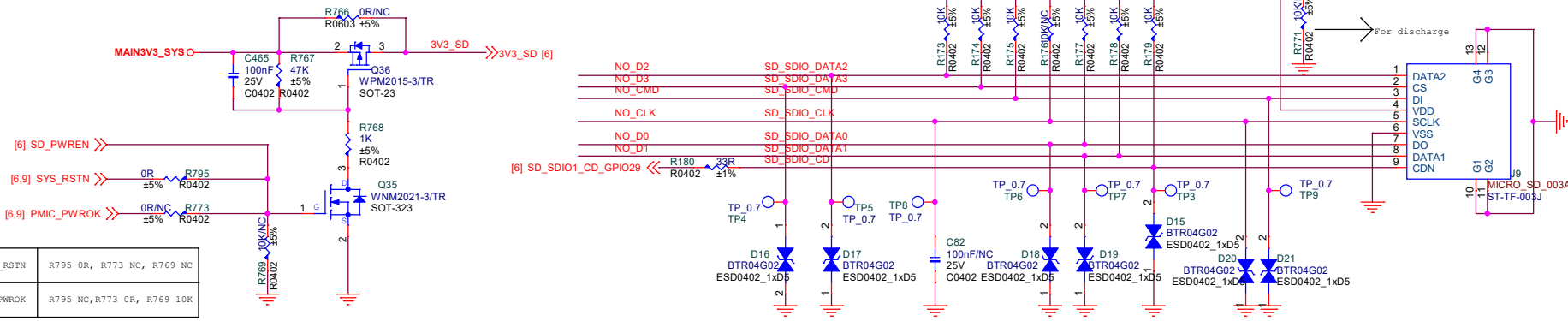
RS485



RS232

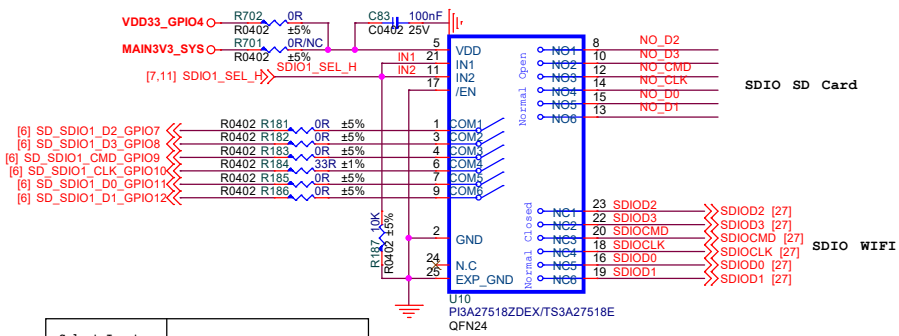


Micro SD Card1



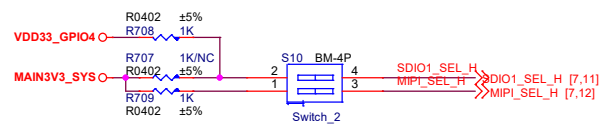
SYS_RSTN	R795 0R, R773 NC, R769 NC
PMIC_PWROK	R795 NC, R773 0R, R769 10K

SDIO Demux



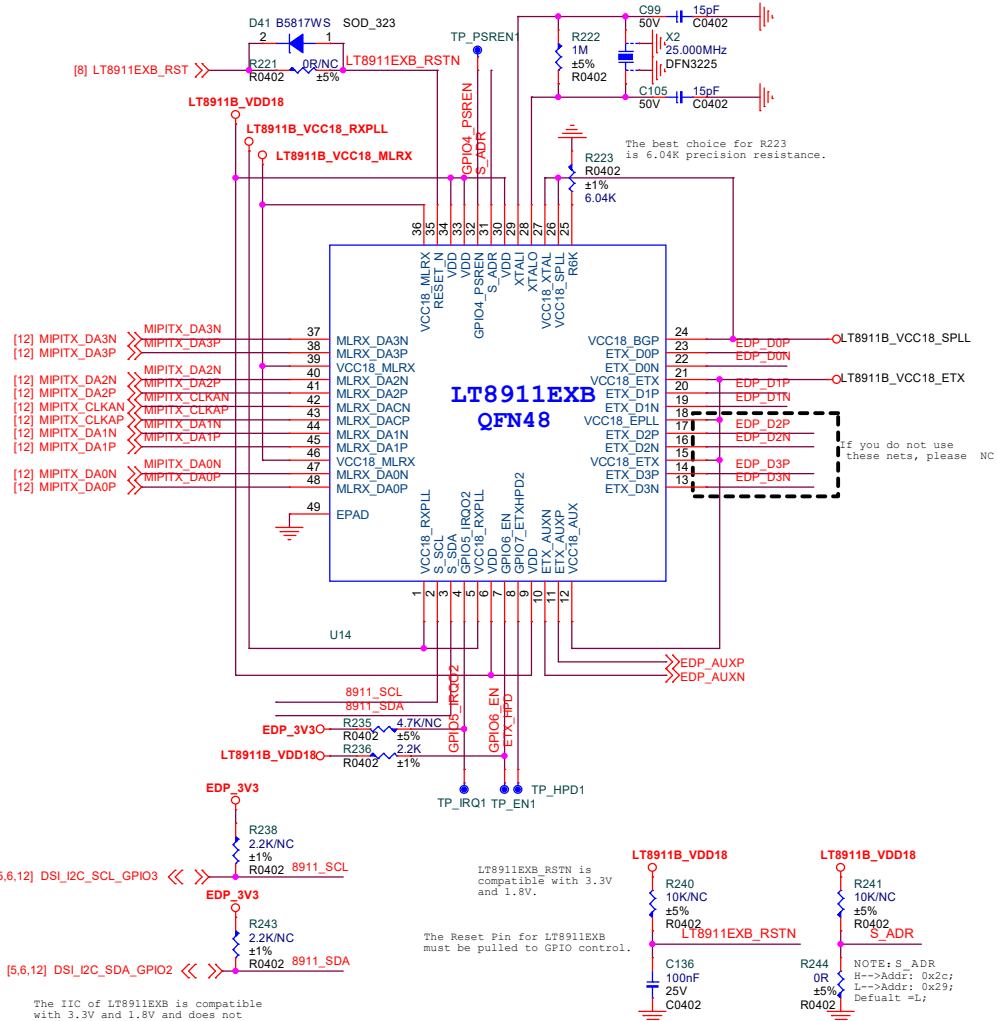
Select Input	Function		
/EN	IN1	IN2	
1	X	X	All Channels are OFF
0	0	0	NC1,2,3 Connected to COM1,2,3 NC4,5,6 Connected to COM4,5,6
0	1	0	NO1,2,3 Connected to COM1,2,3 NO4,5,6 Connected to COM4,5,6
0	0	1	NC1,2,3 Connected to COM1,2,3 NO4,5,6 Connected to COM4,5,6
0	1	1	NO1,2,3 Connected to COM1,2,3 NO4,5,6 Connected to COM4,5,6

SDIO DeMUX Select & MIPI DeMUX Select

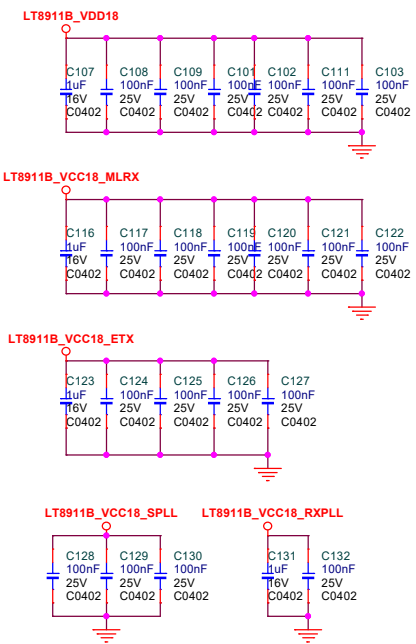


MIPI to eDP

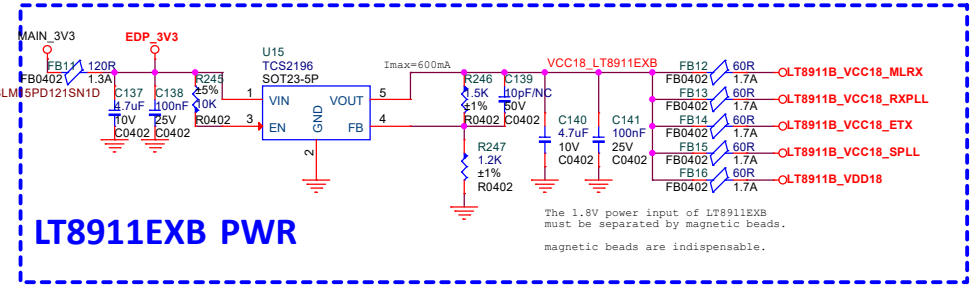
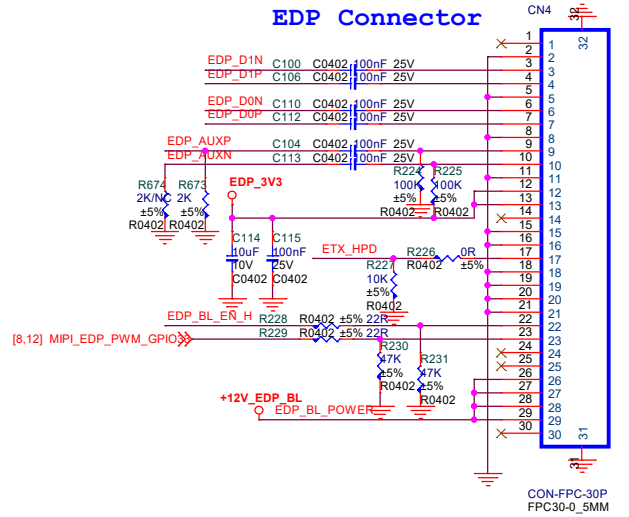
If LT8911EXB_RSTN is connected with pull-up resistance to 1.8V, D41 can be omitted.



De-Couple Cap

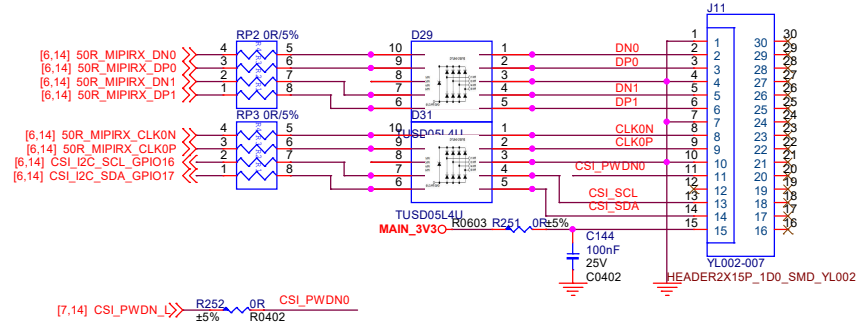


EDP Connector

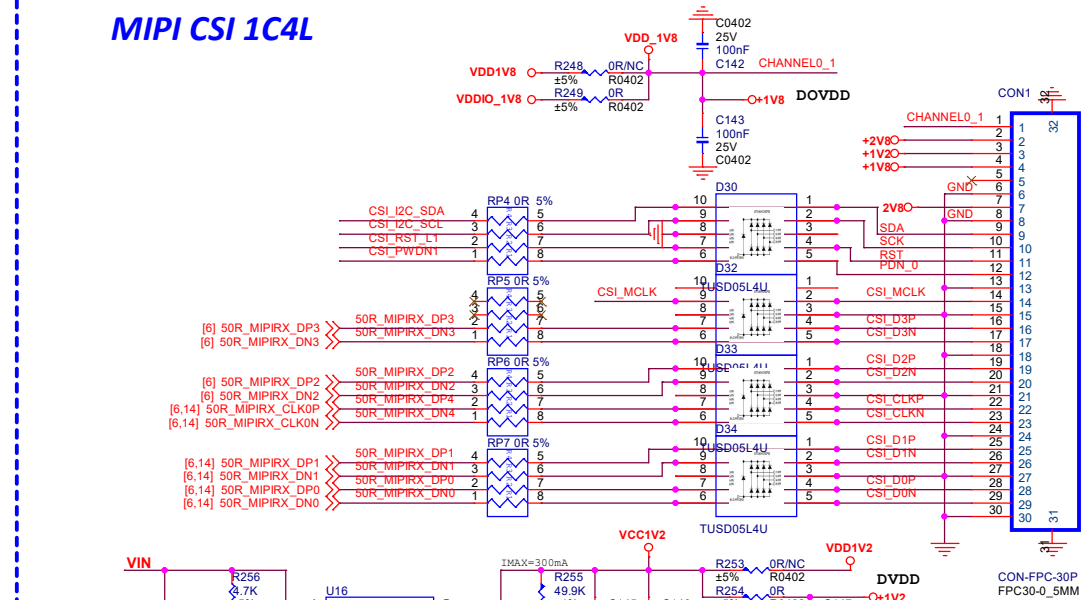


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Title: JH7110_Devkit_MB_V20		
Size: A4	Document Number: MIPI to eDP	Rev: V2.0
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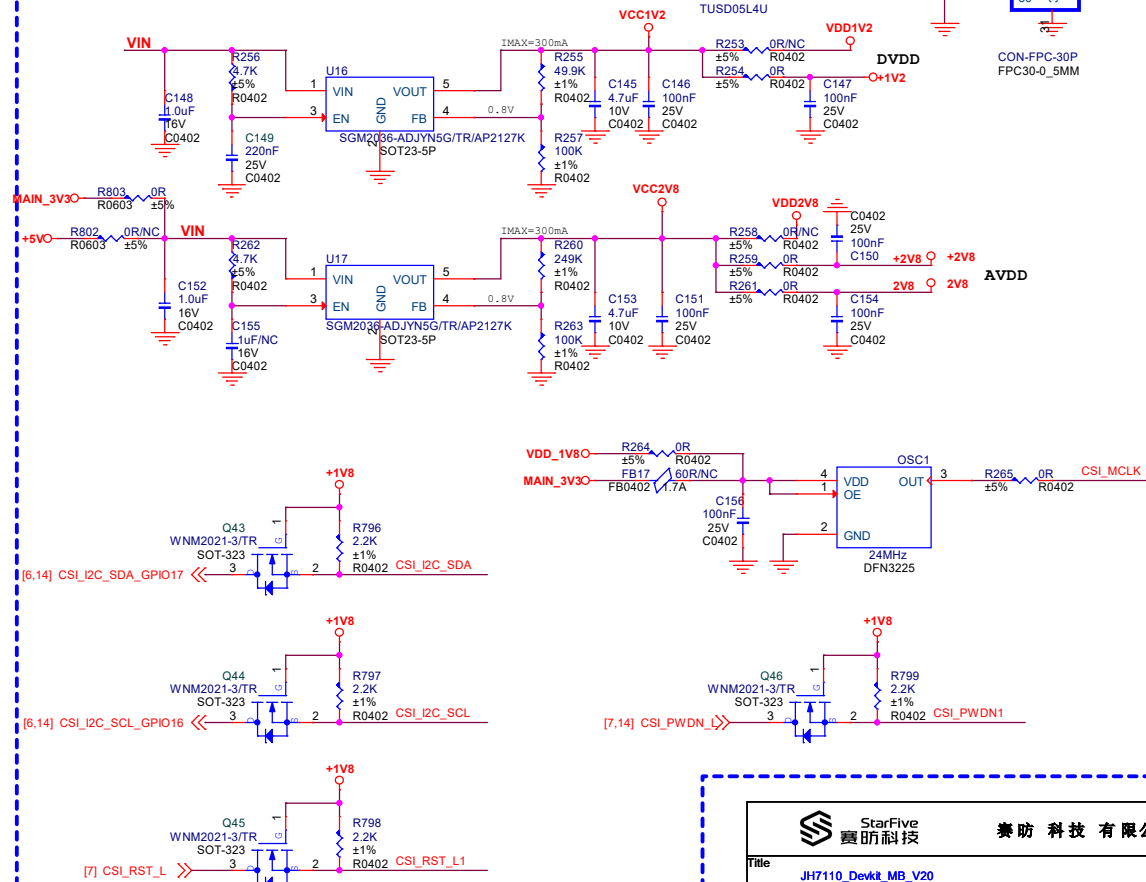
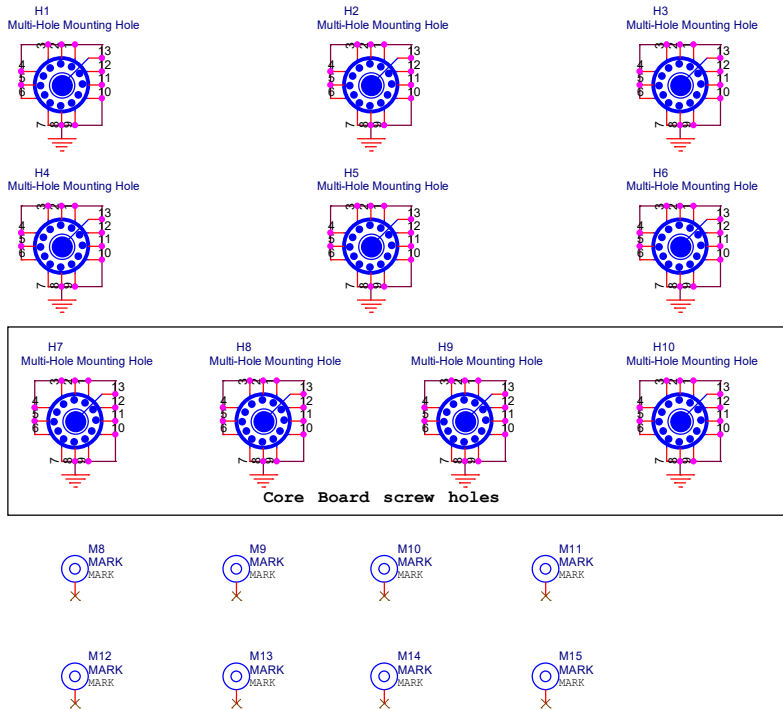
MIPI CSI 1C2L



MIPI CSI 1C4L

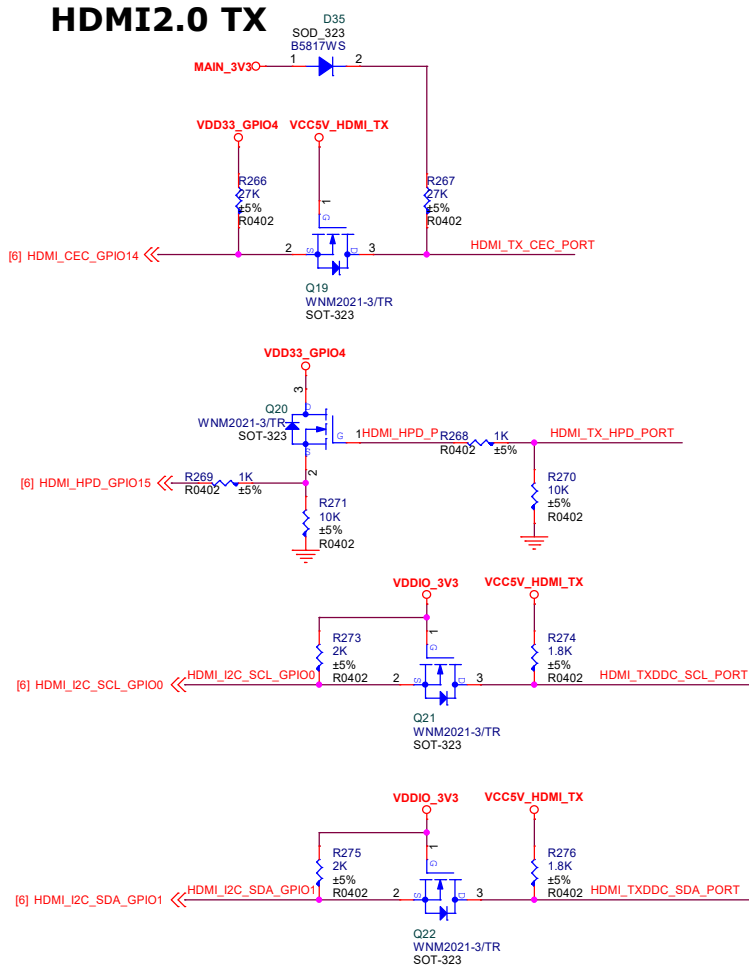


MARK points_screw holes

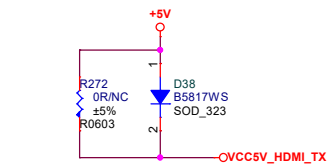
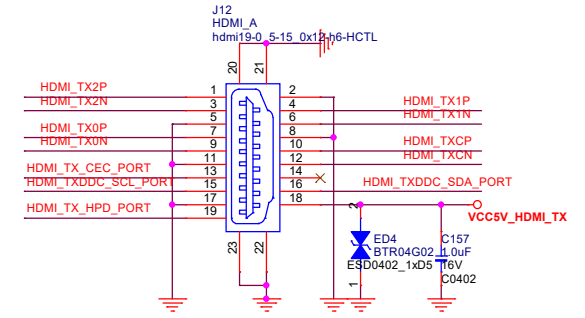
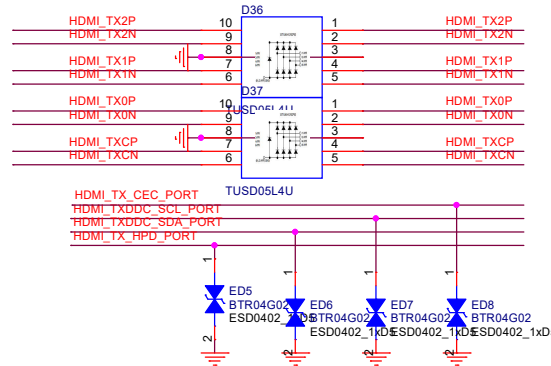


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Title: JH7110_DevKit_MB_V20			
Size: A4	Document: MIPI CSI	Number:	Rev: V2.0
Date: Monday, September 18, 2023	Sheet: 14	of:	27

HDMI2.0 TX



$C_j \leq 0.4 \text{ pF}$



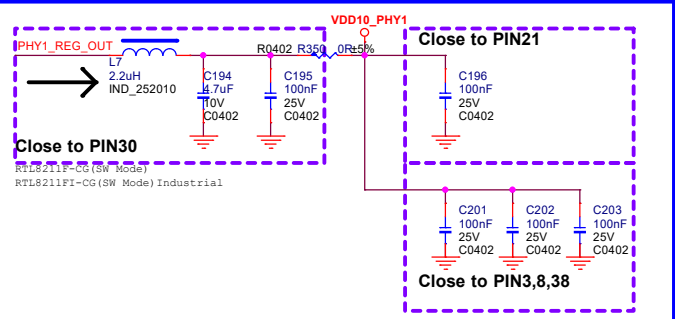
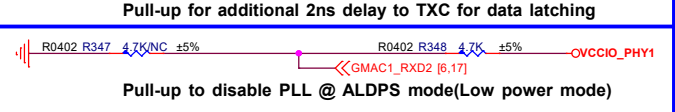
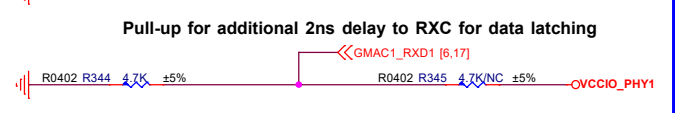
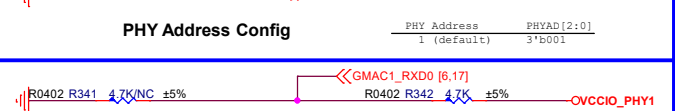
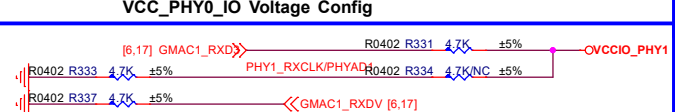
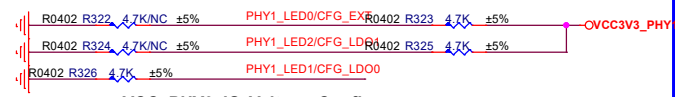
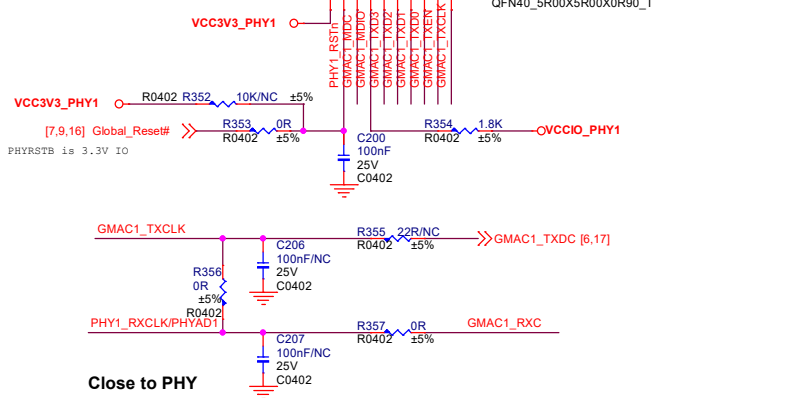
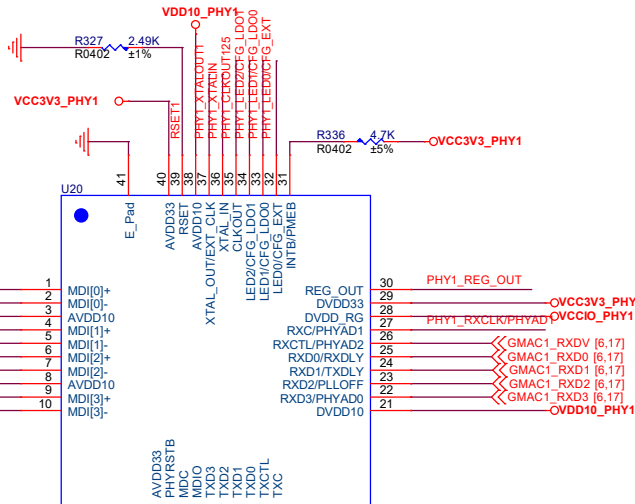
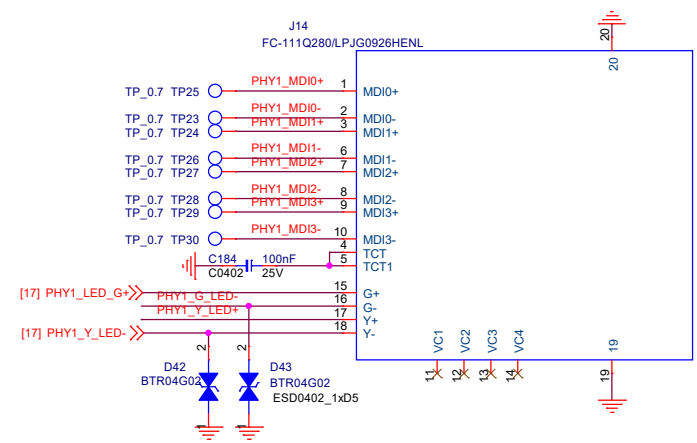
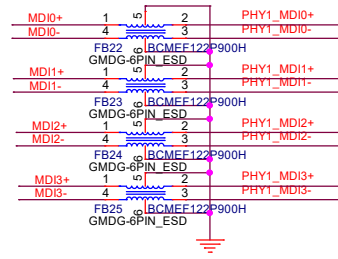
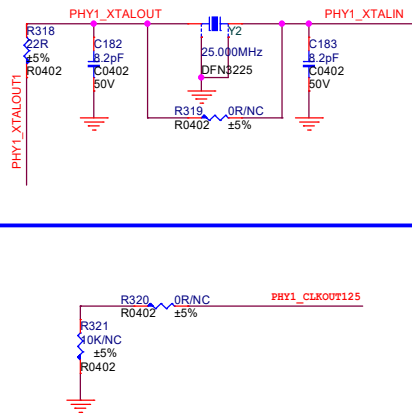
[6] 50R_HDMITX0_Tx2p	HDMI_TX2P_PORT	DLW21SN900HQ2L	20V/280mA	HDMI_TX2P
[6] 50R_HDMITX0_Tx2n	HDMI_TX2N_PORT	CM0805	90OHM/6GHZ	HDMI_TX2N
[6] 50R_HDMITX0_Tx1p	HDMI_TX1P_PORT	DLW21SN900HQ2L	20V/280mA	HDMI_TX1P
[6] 50R_HDMITX0_Tx1n	HDMI_TX1N_PORT	CM0805	90OHM/6GHZ	HDMI_TX1N
[6] 50R_HDMITX0_Tx0p	HDMI_TX0P_PORT	DLW21SN900HQ2L	20V/280mA	HDMI_TX0P
[6] 50R_HDMITX0_Tx0n	HDMI_TX0N_PORT	CM0805	90OHM/6GHZ	HDMI_TX0N
[6] 50R_HDMITX0_Ckp	HDMI_TXCLKP_PORT	DLW21SN900HQ2L	20V/280mA	HDMI_TXCP
[6] 50R_HDMITX0_Ckn	HDMI_TXCLKN_PORT	CM0805	90OHM/6GHZ	HDMI_TXCN

Giga PHY1

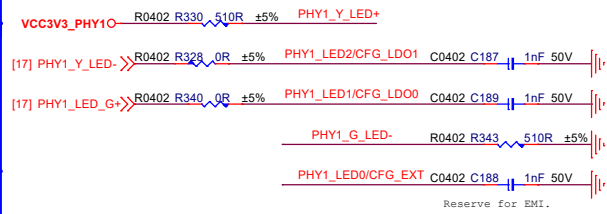
GMAC1_TXD0 [6]
GMAC1_TXD1 [6]
GMAC1_TXD2 [6]
GMAC1_TXD3 [6]
GMAC1_TXEN [6]

GMAC1_TXDC [6,17]
GMAC1_RXD0 [6,17]
GMAC1_RXD1 [6,17]
GMAC1_RXD2 [6,17]
GMAC1_RXD3 [6,17]
GMAC1_RXDV [6,17]
GMAC1_RXC [6]

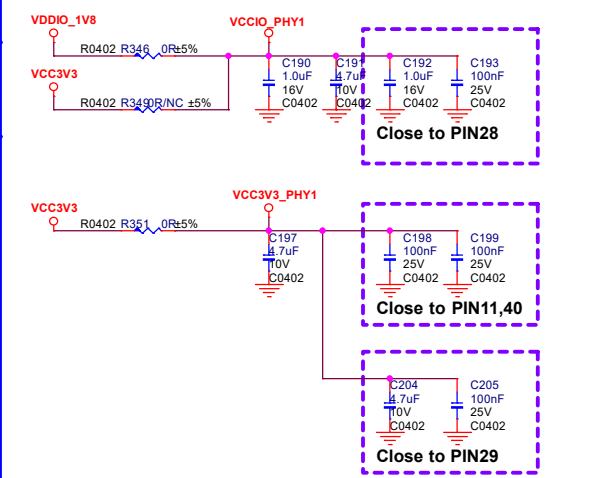
GMAC1_MDC [6]
GMAC1_MDIO [6]



RGMI1 Power Source	CFG EXT	CFG LDO[1:0]
External 3.3V	1'b1	2'b00
External 1.8V (default)	1'b1	2'b10
Internal 1.8V	1'b0	2'b10



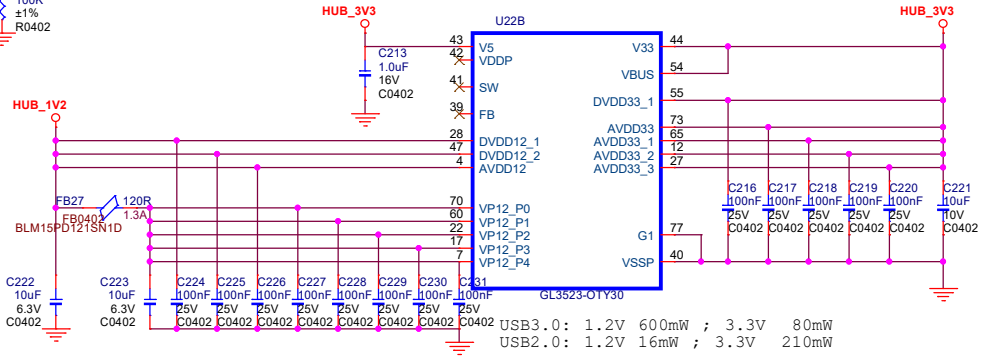
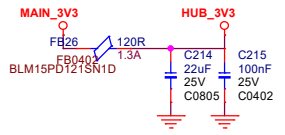
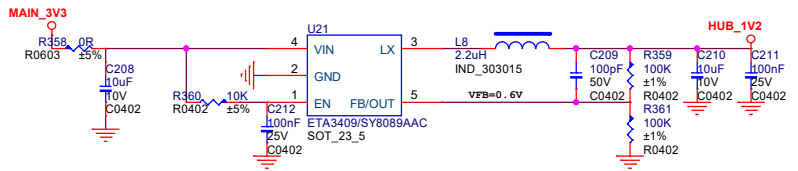
Note:
According to the actual choice of mounted Cannot be mounted at the same time



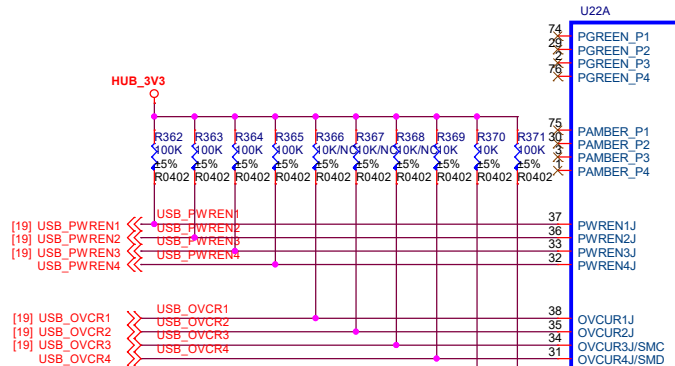
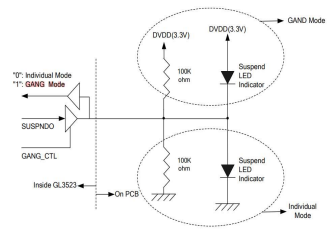
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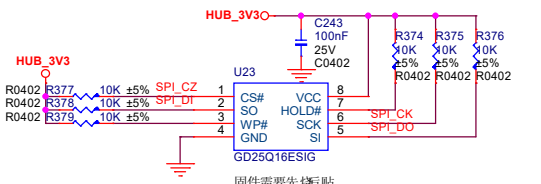
Title		
JH7110_Devkit_MB_V20		
Size	Document Number	Rev
A3	Ethernet_1	V2.0
Date:	Monday, September 18, 2023	Sheet 17 of 27



USB3.0: 1.2V 600mW ; 3.3V 80mW
 USB2.0: 1.2V 16mW ; 3.3V 210mW



Individual Mode



固件需要先烧录

cap should place near the TX Controller (SOC).

AC coupling cap only required on the USB3.X TX data lane, not required for both USB3.X RX and USB2.0 lane. Optional on the RX data lane

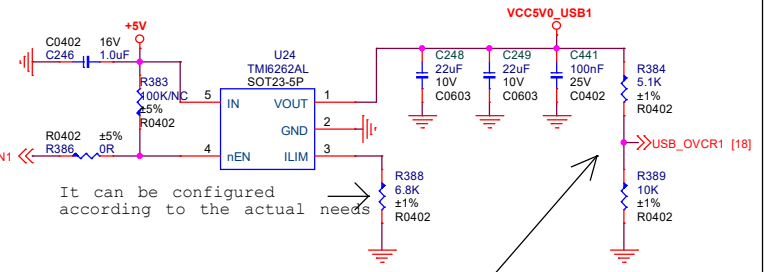
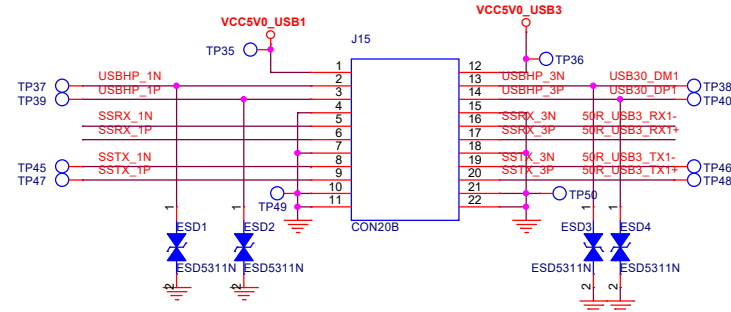
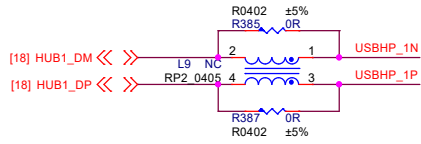
The probe point of the USB3_RX diff pair should place near the hub.

The probe point of the USB3_RX diff pair should place near the hub.

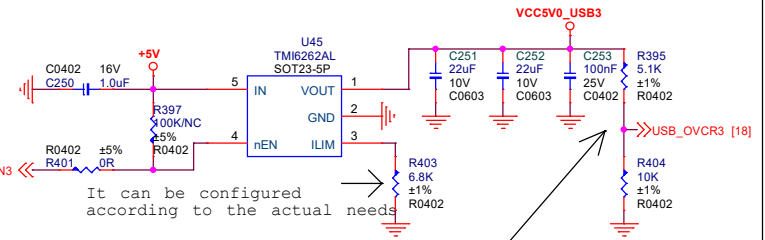
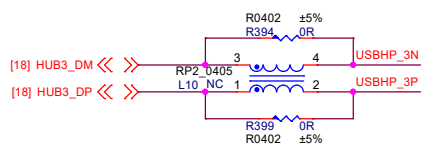
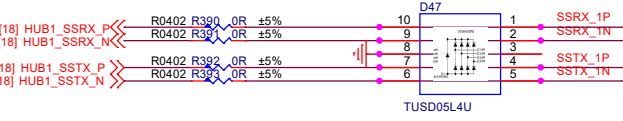
The probe point of the USB3_RX diff pair should place near the hub.

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Title: JH7110_DevKit_MB_V20		
Size: A3	Document Number: USB3.0 HUB	Rev: V2.0
Date: Tuesday, September 19, 2023	Sheet: 18	of 27

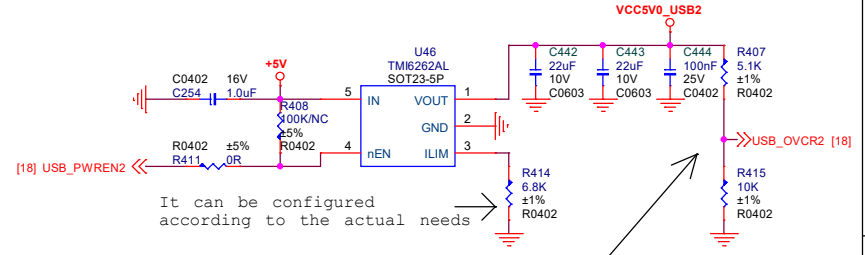
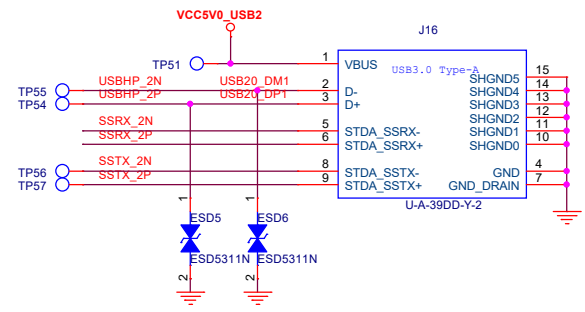
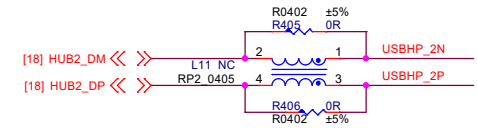
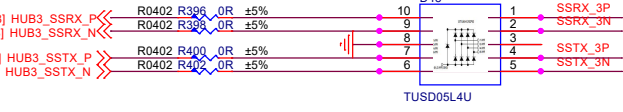
USB_3.0



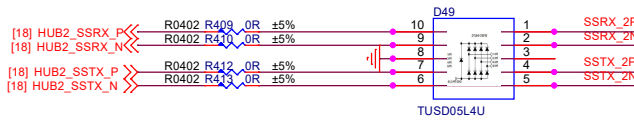
The USB port power supply and its corresponding USB port overcurrent signal can also be isolated by adding a PMOS



The USB port power supply and its corresponding USB port overcurrent signal can also be isolated by adding a PMOS

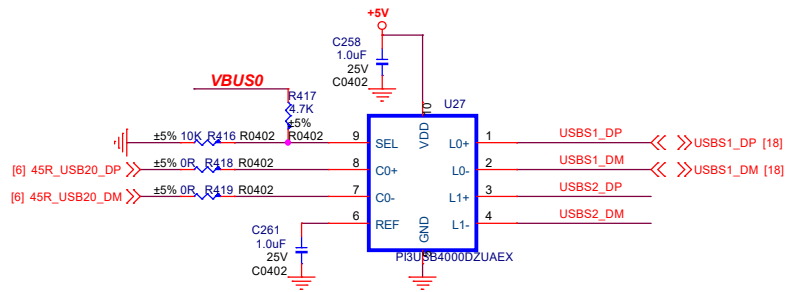


The USB port power supply and its corresponding USB port overcurrent signal can also be isolated by adding a PMOS



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Title: JH7110_DevKit_MB_V20	
Size: A3	Document Number: USB3.0
Date: Monday, September 18, 2023	Sheet: 19 of 27
Rev: V2.0	

USB2.0 DeMUX

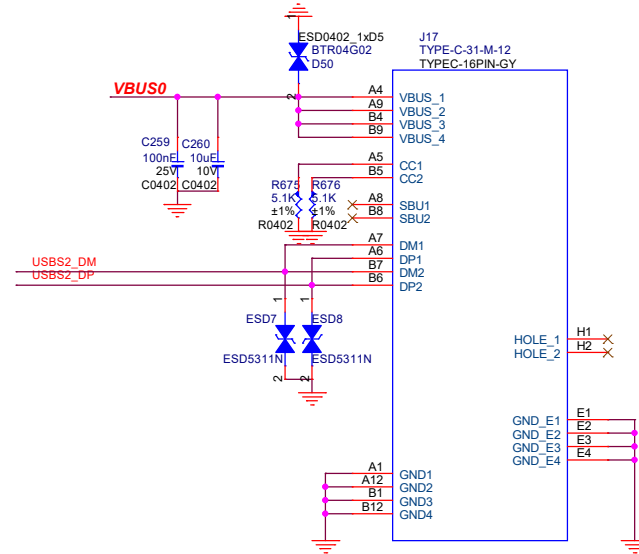


SEL 信号脚 Pin 9:
高电平选择 USB S 2 端;
低电平选择 USB S 1 端

Function	SEL
C0+/- to L0+/-	L
C0+/- to L1+/-	H

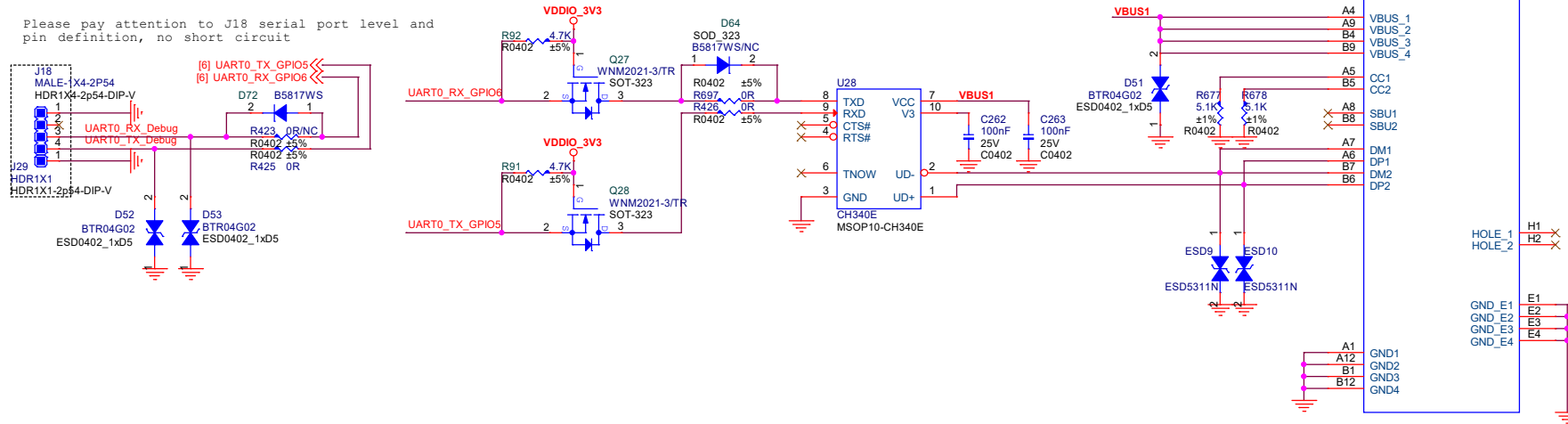
Type-C PROGRAMMING

BOOT MODE: UART



UART0 Debug

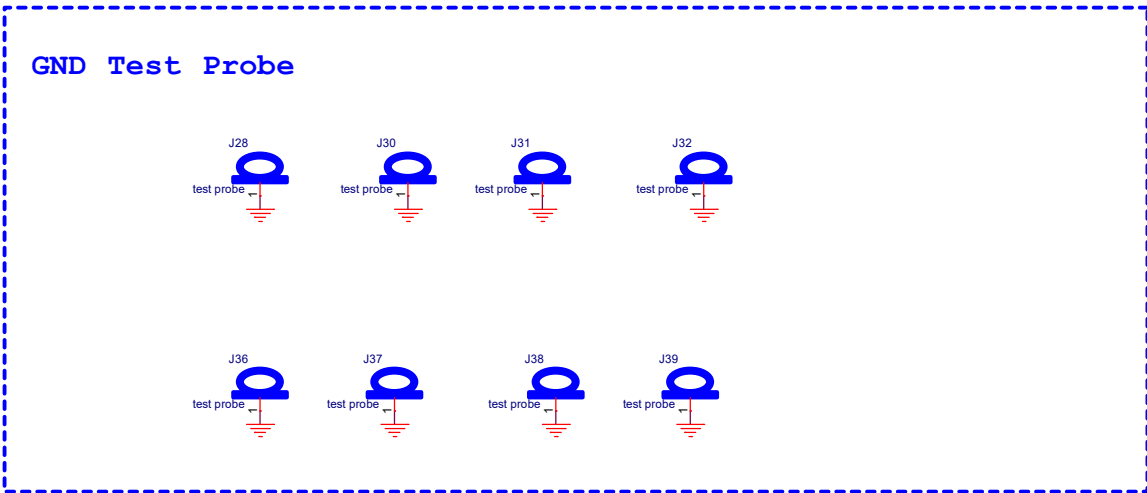
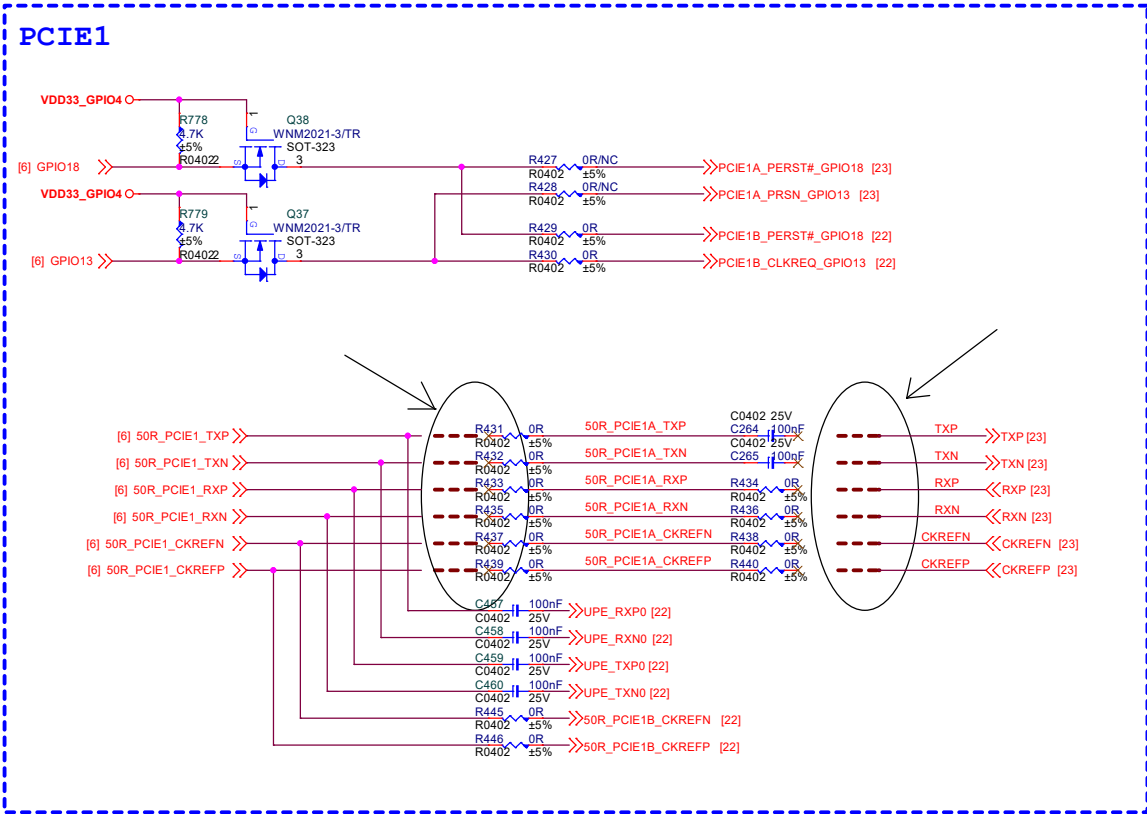
Please pay attention to J18 serial port level and pin definition, no short circuit



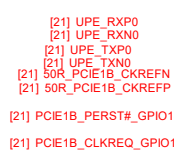
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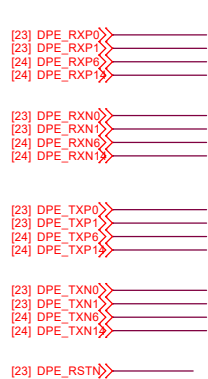
Title JH7110_Development_MB_V20		
Size A3	Document Number USB2.0 Demux & UART0 Debug	Rev V2.0
Date Monday, September 18, 2023	Sheet 20	of 27



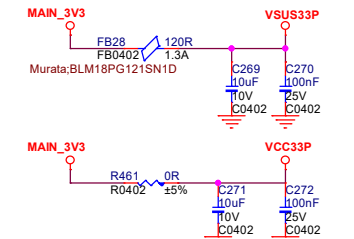
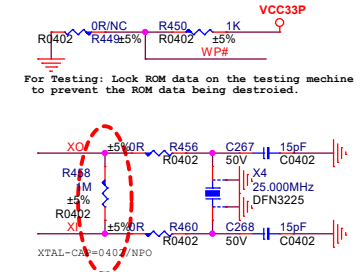
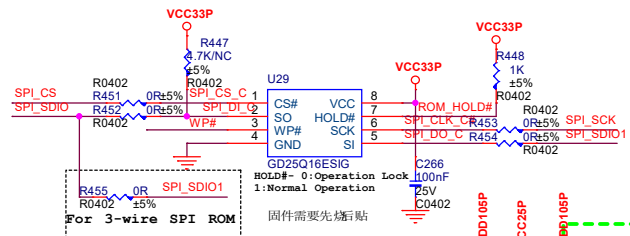
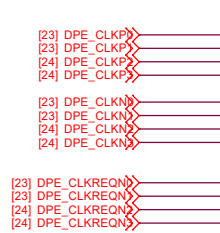
PCIE UPSTREAM



PCIE DOWNSTREAM



PCIE CLOCK

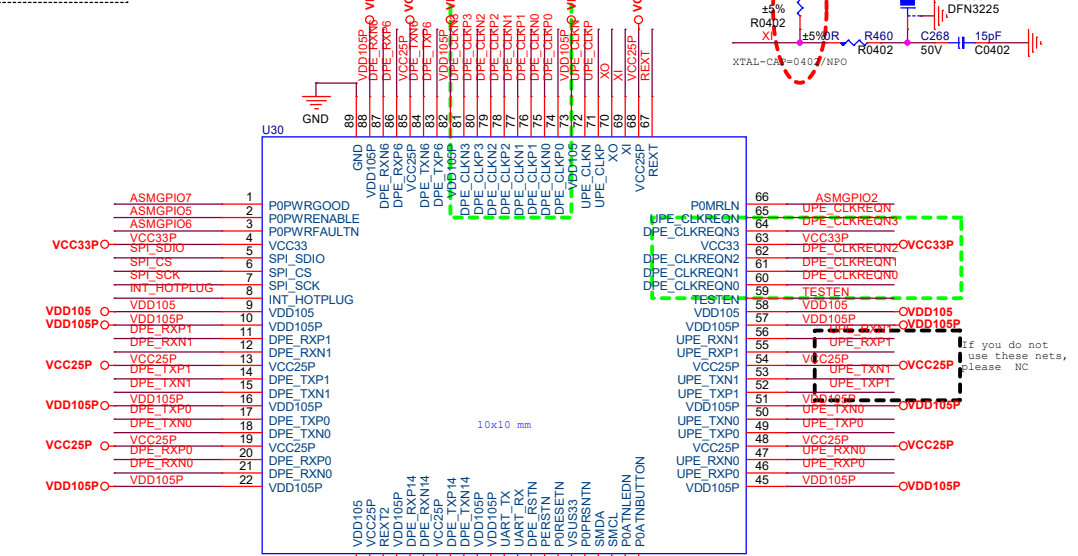
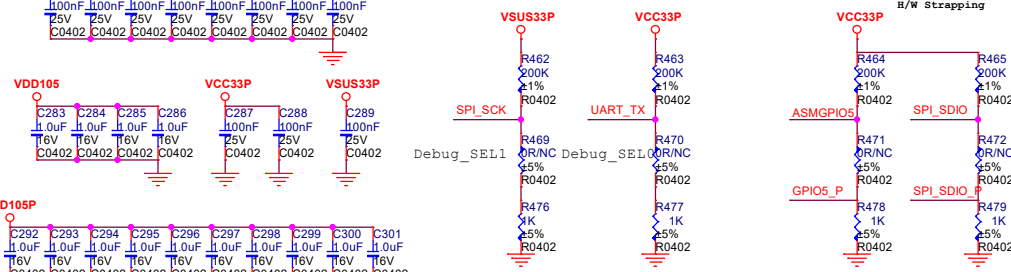


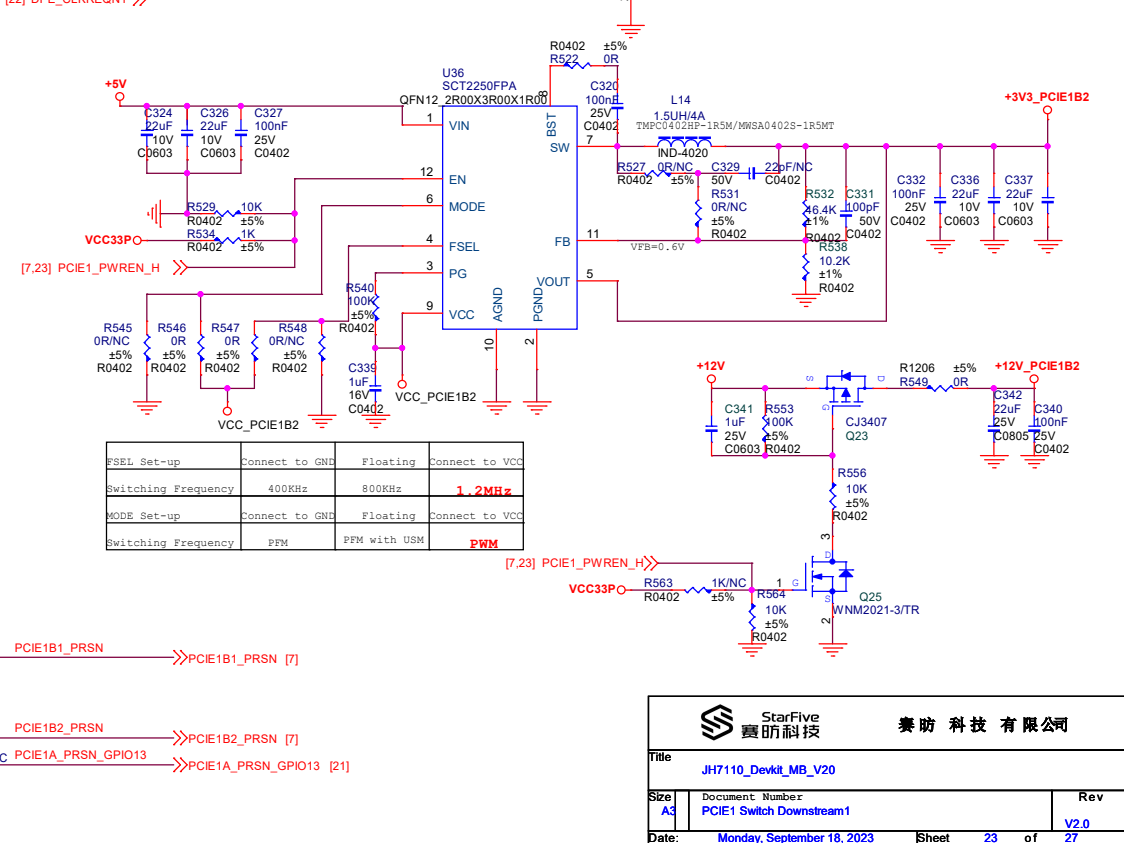
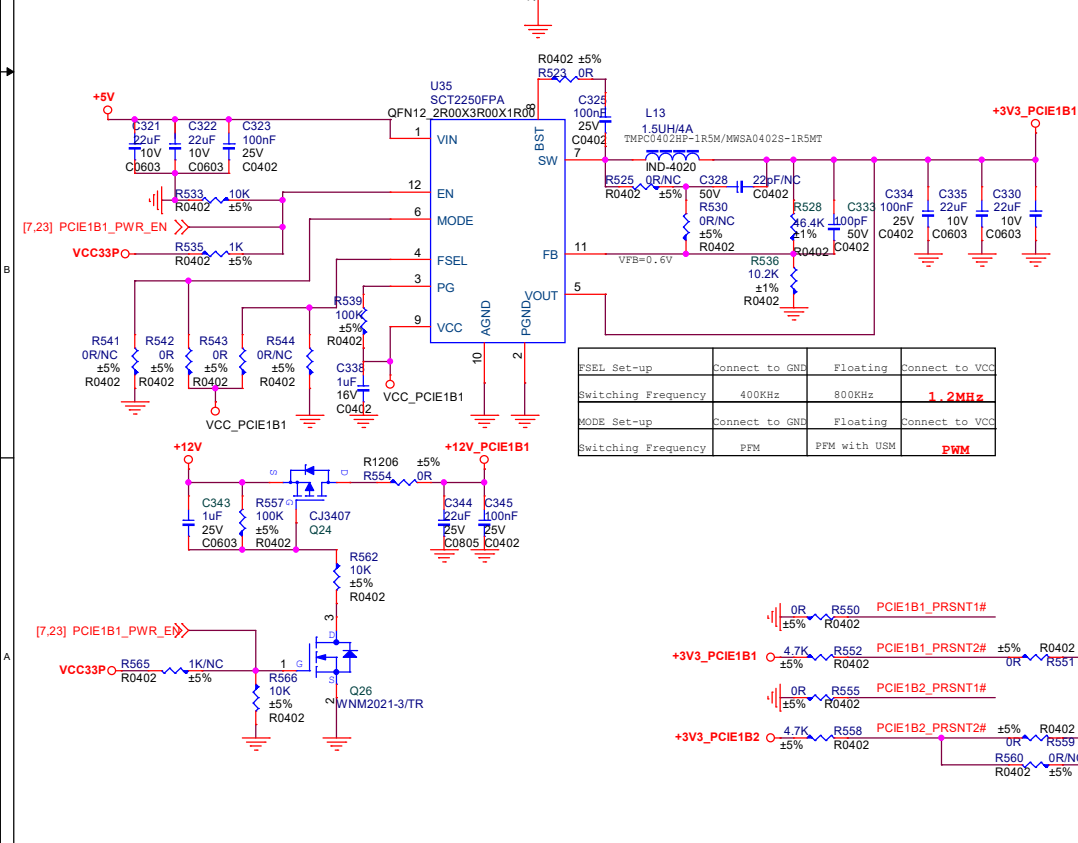
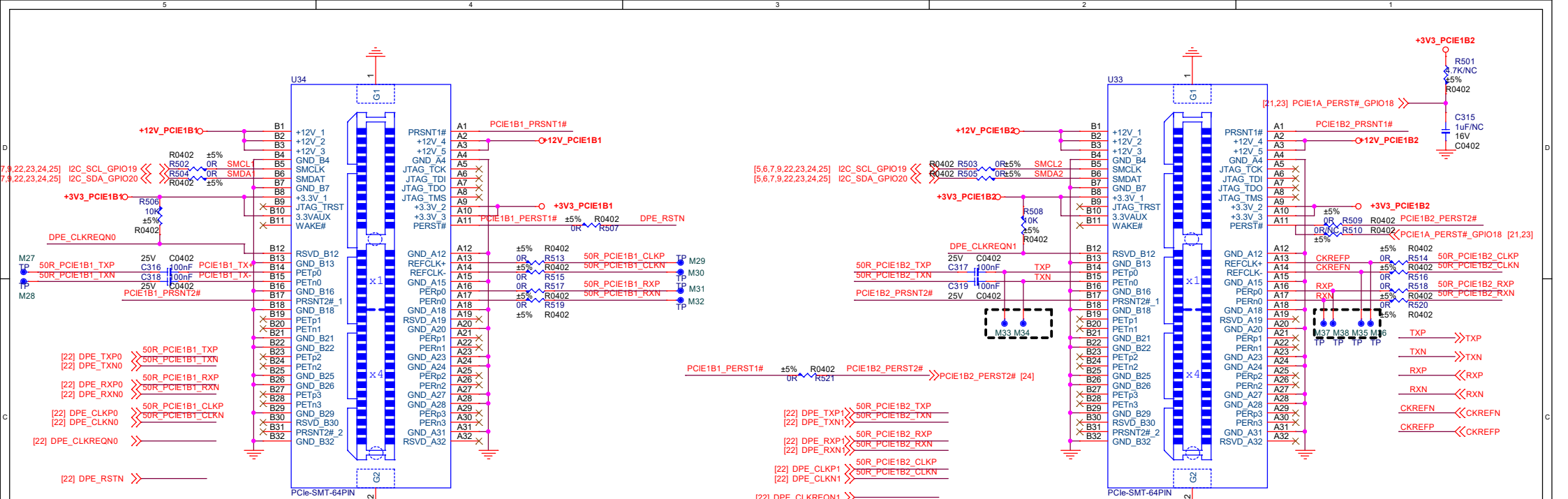
Strapping bit	Upstream Clock
SPI_SCK	0: 100MHz diff 1: OSC
Strapping bit	Downstream Clock
UART_TX	0: 100MHz diff 1: OSC

Strapping bits	LANE0	LANE1	LANE6	LANE14
SPI05, SPI_SDIO				
PECLK Mapping	LANE0	LANE1	LANE2	LANE3
1	1	X1	X1	X1
0	0	X2	X1	X1

Clock mode select: SPI_SCK, UART_TX

ASM1806 PCIe lane configuration:

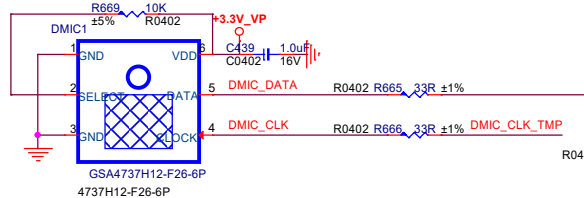
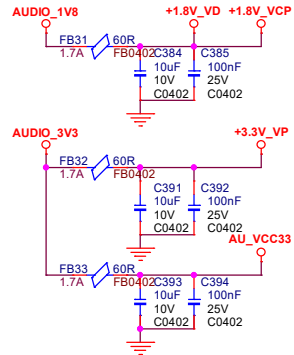




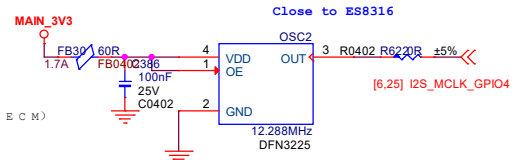
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Title: JH7110_DevKit_MB_V20
 Size: A3
 Document Number: PCIe1 Switch Downstream1
 Date: Monday, September 18, 2023
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Audio ES8316



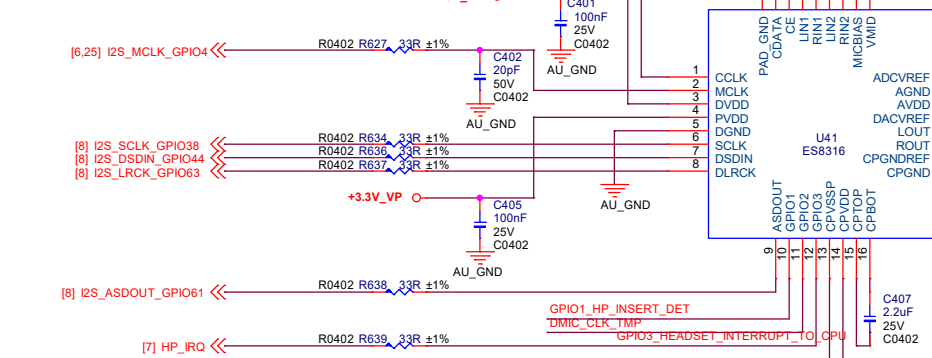
I2S MCLK OSC



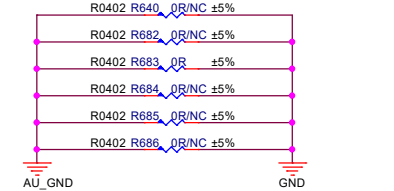
It is recommended that the I2C has clean waveform. Please add the 20pF capacitors between I2C clock route and ground, add 100R series resistor between I2C clock route and IC PIN.

[5,6,7,9,22,23,24] I2C_SDA_GPIO20 << R625 100R
 [5,6,7,9,22,23,24] I2C_SCL_GPIO19 << R626 100R

It is recommended that the I2s clock routes have the same length, if the length of 25 clock is larger than 10cm, please add 30pF capacitors between I2S clock route and ground.



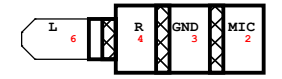
音频地 AU_GND 与系统地 GND 之间采用单点接地方式



这几颗电容靠近芯片放置，电容与芯片之间的走线在同一层走线，不要放置过孔在走线上

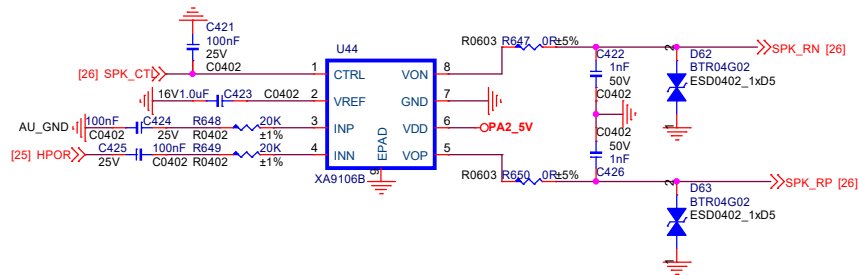
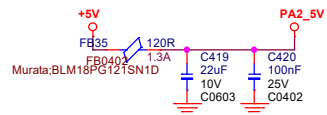
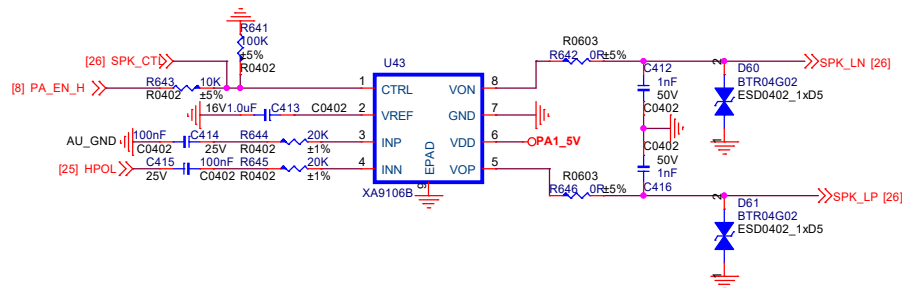
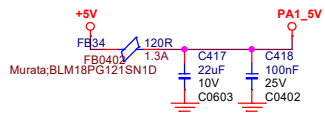
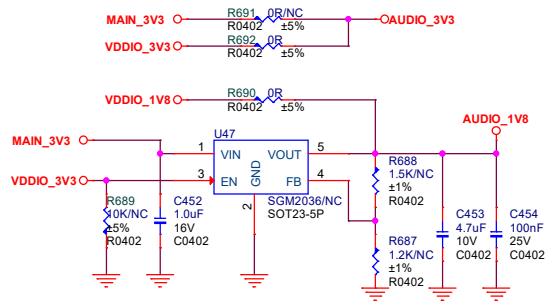
+3.3V_VP, 数字 I/O 电压源
 +1.8V_VP, 数字内核电压源 建议用 1.8V 供电以降低功耗
 +1.8V_VCP, CHARGE PUMP 电压源, 必须用 1.8V 供电
 AU_VCC33, 模拟电压源 建议用 3.3V

推荐使用 LDO 为 ES8316 供电，以取得较好的噪底



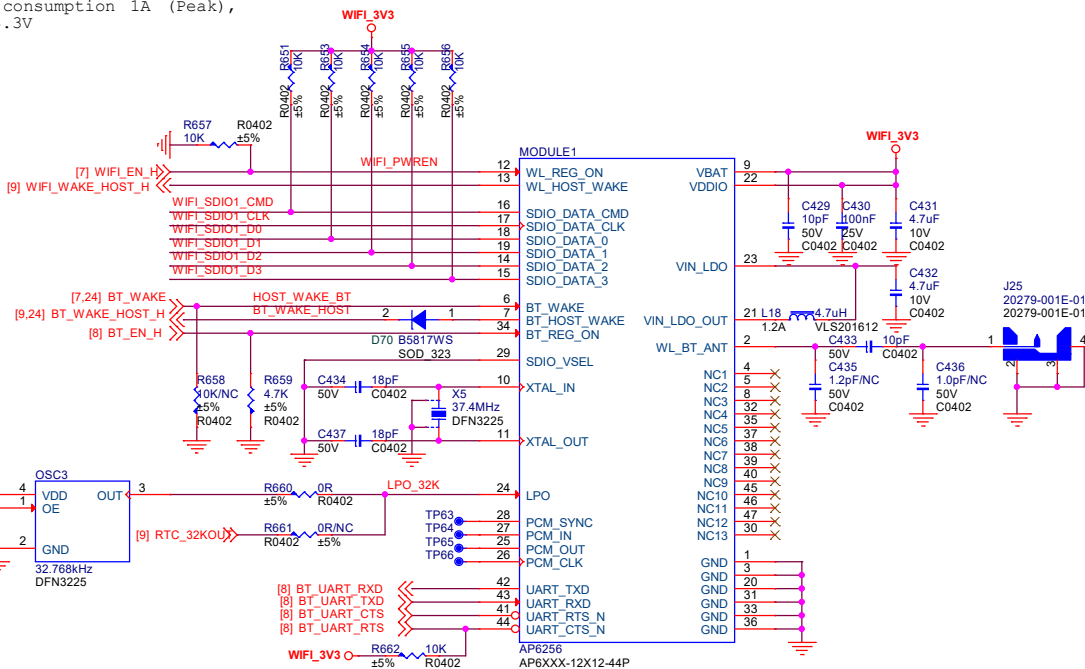
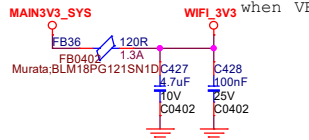
四段式耳机插头美标 (CTIA) 国际标准接线图

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WIFI_BT Module

VBAT current consumption 1A (Peak),
when VBAT = 3.3V



SDIO mode selection pin
1:1.8V(SDIO 3.0/ 2.0), 0 3.3V(SDI O 2.0)

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Title: JH7110_Devkit_MB_V20		
Size: A3	Document Number: AP6256_WIFI/BT_MODULE	Rev: V2.0
Date: Monday, September 18, 2023	Sheet: 27	of: 27